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SEP 77 W F KOSONOCKY, R L ANGLE, J E CARNES N00173-76-C-0980
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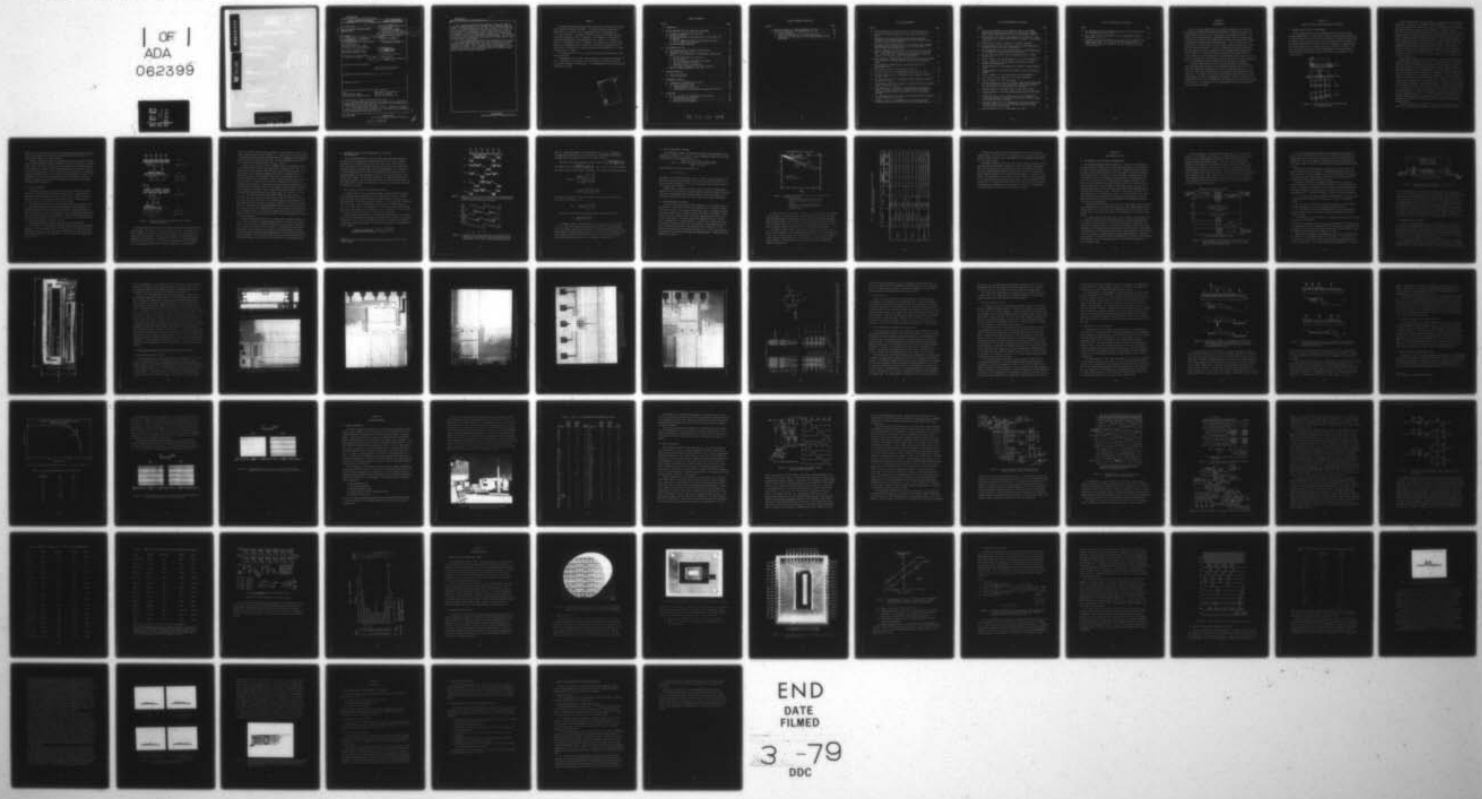

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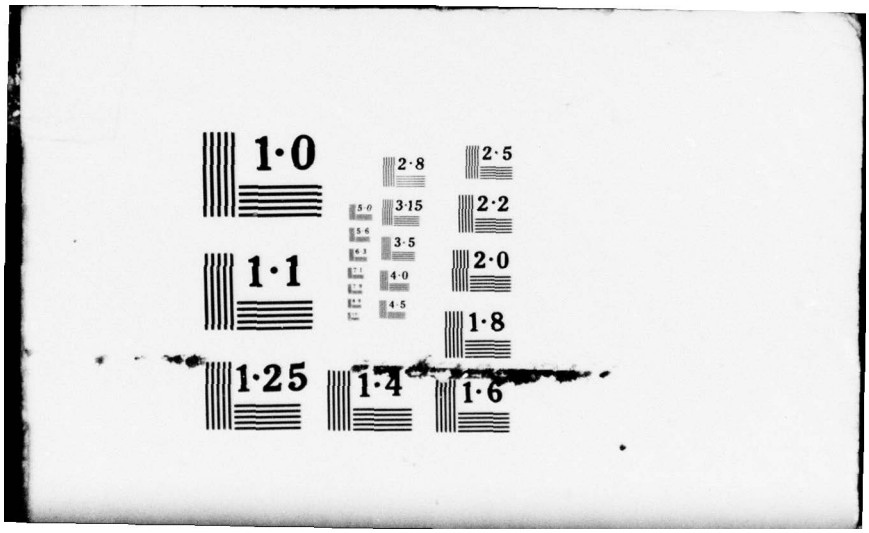
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CCD PAGE READER FOR MAIL-SCANNING APPLICATIONS

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The following new design concepts for construction of a high-speed 2200x96-element TDI-CCD line sensor were developed and demonstrated with a 748x96-element page-reader test chip.

(1) The four-phase electrode-per-bit clock to improve the vertical resolution of the TDI array by a factor of 1.5 was proposed and designed in the 748x96-element page-reader test chip.

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(2) To improve horizontal resolution and achieve the required effective output scanning rate of 8.4×10^7 picture elements (PELs) per second. The 748x96-element TDI array with 0.6 mil x 0.6 mil PELs and built with two-level polysilicon buried-channel CCDs can be read out by two types of 4:1 multiplexed outputs. One side of the array can be scanned-out by four parallel output registers with 2.4-mil stages. This mode of operation was experimentally demonstrated. The other side of the array can be scanned-out by two pairs of 2:1 multiplexed output registers with 1.2-mil stages.

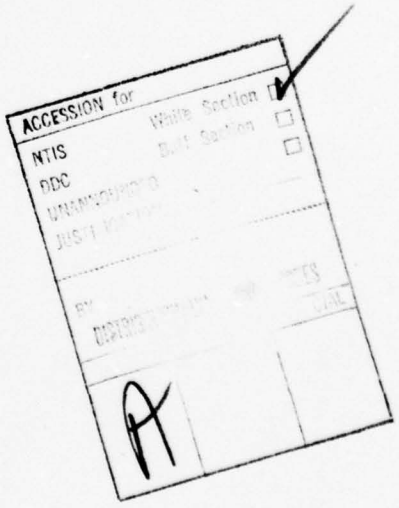
(3) A new charge-gating structure was incorporated in the layout of the 748x96-element page-reader test chip to perform the 4:1 multiplexing of the output of the TDI array before four parallel output registers are loaded. Also a temporary line storage register is used between the multiplexer and the output registers to facilitate high-speed loading of the output registers.

PREFACE

This Final Report was prepared by RCA Laboratories, Princeton, New Jersey, under Contract No. N00173-76-C-0980. It describes work performed from 15 March 1976 to 15 May 1977, in the Integrated Circuit Technology Center, J. H. Scott, Director. The project Supervisor was K. H. Zaininger, and the Principal Investigator is W. F. Kosonocky. Other Members of the Technical Staff who participated in this program were R. L. Angle, J. E. Carnes, D. J. Sauer, F. V. Shallcross, and P. A. Levine. The coding of the chip layout was done by D. Allesandrini and G. M. Meray; the devices were processed by W. S. Romito and L. M. Bijaczyk; the waveform generator was designed by A. R. Criado and built by C. Y. Tayag.

The Technical Monitor is F. C. Martin of Naval Ocean Systems Center, San Diego, California.

The manuscript of this report was submitted by the authors on September 7, 1977. Publication of this report does not constitute the Navy approval of the report's findings or conclusions. It is published only for the exchange and stimulation of ideas.



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SECTION I

INTRODUCTION

There is a future requirement for an optical scanning device to be used for Electronic Message Service (EMS) systems which is capable of reading up to 20 pages (8-1/2 in. x 11 in.) per second, with 5-mil element resolution. To achieve the above reading rate, a high-speed CCD line sensor is needed, which is capable of an overall serial sample rate of 84 MHz, with about 100:1 dynamic range at paper subcombustion illumination levels. Also, it is desirable for this device to be on one chip (i.e., not require butting of chips) and to have 2200 line-resolution elements. Since the commercially available 1728-element CCD line sensor is rated for operation with the maximum serial sampling rate in the range of 1 to 10 MHz, the general objectives of the work under this contract were to develop and demonstrate new CCD image sensor concepts that will lead to an increase in the line-sensor scanning rate about one order of magnitude, and to an improvement in optical sensitivity by two orders of magnitude.

To achieve simultaneously both of the above performance improvements, a high-speed 2200-element CCD line sensor design was proposed with 96 TDI (time-delay and integration) elements and 4:1 to 8:1 multiplexed serial outputs. To demonstrate these new CCD image sensor techniques both experimentally and with respect to the feasibility of fabricating a 2200x96-element TDI-CCD line sensor, a page-reader test chip was designed and fabricated. The major feature of the page-reader test chip is a 748x96-element TDI-CCD line sensor with 4:1 multiplexed serial outputs. The operation of this 748x96-element sensor was demonstrated with pulsed optical inputs.

SECTION II

DESIGN TRADE-OFFS FOR CCD HIGH-SPEED PAGE READER

A. SYSTEMS FOR HIGH-SPEED CCD PAGE READER

The long-range objective of the high-speed CCD line reader for mail-scanning applications is to have 1728 or 2200 horizontal picture elements and, for improved sensitivity, 96 TDI vertical elements. To satisfy the requirement of reading up to 20 pages per second, this line reader should be capable of a horizontal scanning rate of 84 MHz. Since it is difficult to provide drivers for clocking the CCD output register much above 21 MHz, the readout of this array must involve some form of output multiplexing. The four different systems with 4:1 multiplexed outputs considered for this purpose are illustrated in Fig. 1.

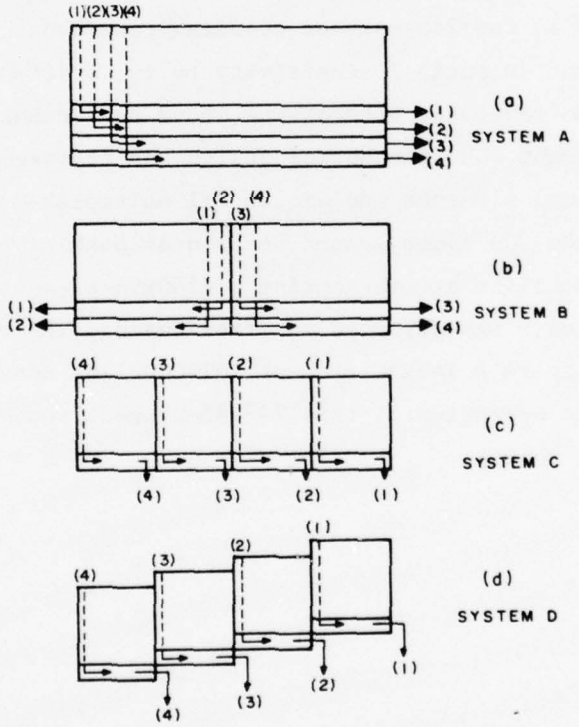


Figure 1. System organization for TDI array with 4:1 multiplexed output.

System A shown in Fig. 1(a) represents the approach with 4:1 multiplexed output that is capable of the highest horizontal resolution. In this system every four adjacent PELs of the sensor array are transferred into four adjacent horizontal CCD output registers as shown in Fig. 2. System B, shown in Fig. 1(b), is split into two sections, each having a separate set of 2:1 multiplexed registers. System C, shown in Fig. 1(c), provides the output signals from four simultaneously scanned output registers. This system represents four smaller sensors in adjacent locations designed to form a single and continuous (in the horizontal direction) optical sensor. System D, see Fig. 1(c), was suggested by Frank Martin of Naval Ocean Systems Center. This system is similar to System C, but is designed with each adjacent section (from right to left) with one additional line of TDI delay. In this system a sequential reading of sections 1, 2, 3, and 4 provides a readout of one continuous line of the TDI sensor array.

A more detailed description of the 4:1 and 2:1 output multiplexing used in Systems A and B is given in Section III. The main advantage of using such horizontal output multiplexing in the design of CCD image sensors is that it allows an increase in the horizontal resolution without the requirement of a simultaneous decrease in the stage length of the output register. This, however, also imposes a trade-off between the improvement in the horizontal resolution and a limitation on the maximum clock frequency at which the output resister can be operated with low transfer losses. This loss in transfer efficiency due to the higher order of horizontal output multiplexing is due to the proportionally longer gates in the output register. Although an exact analysis of the frequency response of buried-channel CCDs as a function of gate length, L, is not available, the upper clock frequency at which the transfer loss becomes significant, i.e., falls in the range of 10^{-5} to 10^{-4}, is expected to be inversely proportional to L^2 or L^3. The L^2 dependence should apply when the dominant transfer mechanism is thermal diffusion of free carriers. The L^3 dependence is expected if the charge transfer is controlled by drift-aiding fringing fields.

The main advantage of an approach such as that used in Systems C and D is that it is not limited by the frequency response of the output registers.

However, at the same time this form of output multiplexing imposes the restriction that the length of the picture in horizontal direction be equal to the length of one stage of the output register.

Finally, a compromise between the improvement in the horizontal resolution and the maximum allowable frequency response is achieved in System B, as shown in Fig. 1(b). This type of splitting of the imager into two parallel sections can be used also to achieve an 8:1 multiplexed output in the form of two sets of 4:1 multiplexed outputs. Such an approach may be desirable if the frequency response of System A is too low to satisfy the required effective serial output scanning rate of 8.4×10^7 PELs per second, and the construction of System B imposes too-small feature length for the design of the dual 2:1 horizontally multiplexed output registers.

B. CCD GATE STRUCTURES

The four basic CCD gate structures that have been considered for implementation in the page-reader systems are shown in Fig. 2. These CCD gate structures will be referred to as *single polysilicon CCD* shown in Fig. 2(a), *standard two-phase CCD* shown in Fig. 2(b), *offset-gate CCD* illustrated in Fig. 2(c) and *triple polysilicon CCD* shown in Fig. 2(d).

The single polysilicon CCD is the technology used in the construction of the commercially available RCA 512x320 frame-transfer CCD image sensor. The CCD gates are formed by selectively doped polysilicon fingers separated by opposite conductivity, lightly doped gaps. At RCA, a three-phase gating structure is used with the single poly technology. For this type of construction, the minimum stage length, L, is given by $L = 6\ell$ where ℓ is the minimum feature for a single polysilicon CCD which is 1.2 mil.

The standard two-phase CCD (see Fig. 2(b) has a stage length of $L = 4(\ell + r)$, where ℓ is the minimum definable feature, and r is the alignment tolerance. For our standard device, $\ell = 0.2$ mil and $r = 0.1$ mil which gives a stage length $L_{min} = 1.2$ mil. The highest density devices fabricated at RCA Laboratories using this technology had $r = \ell = 0.1$ mil, and had stage length $L_{min} = 0.8$ mil.

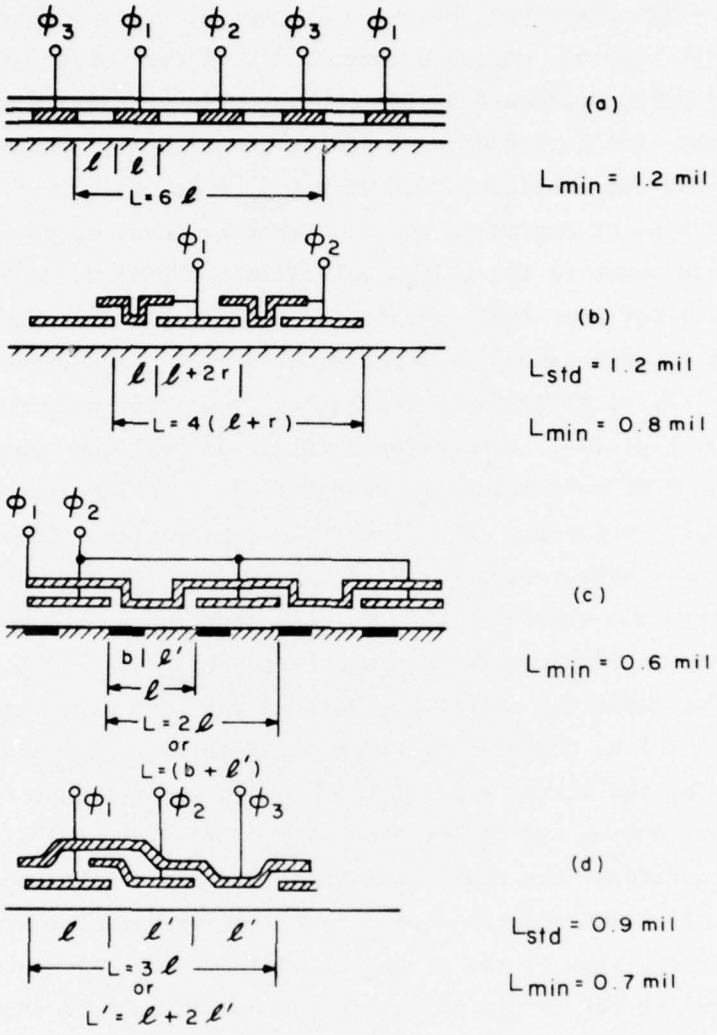


Figure 2. CCD gate structures considered for the systems illustrated in Fig. 1.

The offset-gate CCD [see Fig. 2(c)] probably represents the highest density CCD technology. The offset gate CCD is a two-phase device in which one clock phase is applied to one level of polysilicon and the other clock phase to the other level of polysilicon. Thus, in this technology each polysilicon gate represents one half-stage of a two-phase CCD register. The limiting packing density of these devices for a given process depends mainly on the alignment of the "offset masks" which form the barrier regions with the polysilicon

gates. The barrier regions, having a length, b, are used here to isolate the charge storage regions, having a length, ℓ'. A test array of offset gate CCD's is currently being processed at RCA Laboratories to demonstrate the feasibility of this process for buried-channel CCD's, and also to demonstrate that with this process we can fabricate CCDs with L_{min} = 0.6 mil.

Another type of device in which a separate level of polysilicon is used for each clock phase is the triple polysilicon CCD shown in Fig. 2(d). Although we have not processed a device of this type at RCA Laboratories, it is very similar to our standard two-phase CCD's with one additional level of polysilicon used as a field-shield channel stop. Our original concept of System A (see Fig. 1(a)) considered a triple polysilicon construction in which the first level of polysilicon is used for the transfer gates between the parallel output registers. The first triple polysilicon CCD reported by Bell Laboratories was constructed with 1.2 mil stages. We feel, however, that with this technology one should be able to make three-phase CCD's with 0.9 mil stages and the minimum practical stage length L_{min} = 0.7 mil for ℓ = 0.3 and ℓ' = 0.2. One important difference between the gate structure shown in Fig. 2(a) and (b) as compared to those shown in Fig. 2(c) and (d) is that in the first case, the actual size of the storage wells is not dependent on the mask alignment during the device processing. However, the size of the storage wells and, therefore, the charge-handling capacity of the second type of devices (Figs. 2(c) and (d)) depends directly on the precision of the mask alignment. Therefore, what is the practical minimum stage length for the offset gate CCDs and for the triple polysilicon CCDs can only be determined by actual processing experience.

Another unique characteristic of the offset gate and triple polysilicon CCDs is that to achieve the maximum packing density in the TDI array, these devices can be made with a large gate length for the first level of polysilicon, a smaller gate length for the second, and (if applicable) third level of polysilicon. These later gates are formed in the spaces between the first-level gates and their nominal sizes depend mainly on the practical limitation in mask alignment. How the MTF rolloff will be affected by using devices with unequal gate lengths for the TDI array is analyzed in the following section.

C. GENERALIZED ANALYSIS OF MTF ROLLOFF DUE TO TIME DELAY AND INTEGRATION

An inherent mechanism which will cause MTF degradation when using the TDI mode of line imaging occurs because the image is moving at a constant velocity while the collecting potential wells move with a "jerky" motion. Thus, the center of the collecting well will move relative to the image with a periodic motion, falling behind, and then jumping ahead, etc. The degree of the MTF degradation due to this effect depends upon the details of the clocking scheme, the gate dimensions as well as the spatial frequency of the pattern being imaged. The following discussion is a generalized analysis of the contrast transfer function (CTF, appropriate for square wave patterns) for electrode-per-bit clocking with unequal gate lengths and three-phase clocking for unequal gate lengths.

1. CTF for Ripple Clocking (Electrode-per-Bit Clock)

As shown in Fig. 3, this discussion assumes a generalized electrode-per-bit* clocking scheme consisting of pairs of gates, one of length L_1 and the other of length L_2, in which p packets are stored under p + 1 gates. Each gate consists of a storage region and a barrier. P + 1 clocks would be required for this scheme. Figure 3 illustrates the progress of a charge packet for p + 1 = 4. After three clock transistions ($t = t_4$), each packet has moved one gate ahead - one quarter of a full stage. Thus, it takes p(p + 1) clock transitions to move the charge pattern to the right one full stage.

Figure 4 shows the position of the collecting wells relative to the moving image (i.e., the reference is assumed to be moving with the image) as a function of time for p + 1 = 4. Six time periods are shown. The light pattern shown corresponds to the Nyquist limit. The relative speed between a stationary well and the image is

$$\frac{\text{length of full stage}}{\text{time to transit full stage}} = \left(\frac{(p+1)\ \frac{L_1 + L_2}{2}}{p(p+1)\ \Delta t} \right)$$

*Other terms used to describe the electrode-per-bit clock are bit clock and ripple clock.

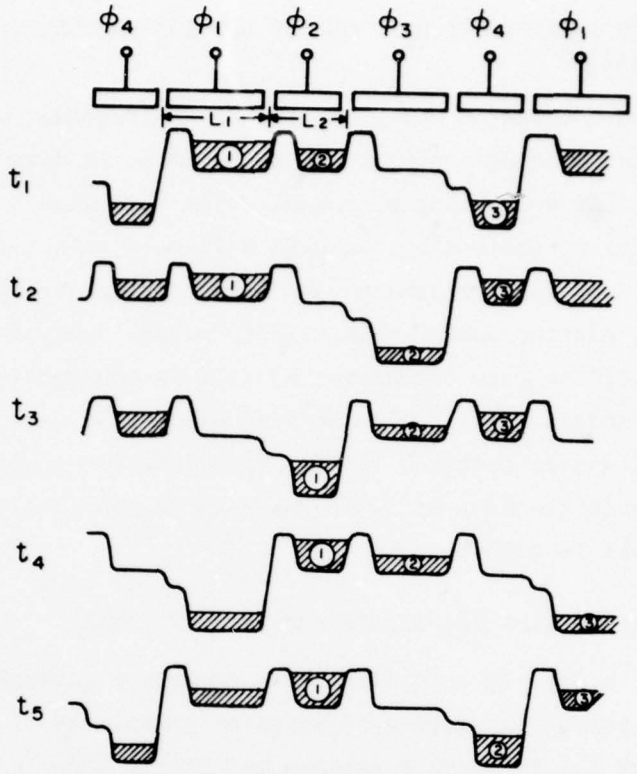


Figure 3. Operation of a TDI array with four-phase electrode-per-bit clocking, illustrating the presence of the three variable sizes of PELs for each four electrodes.

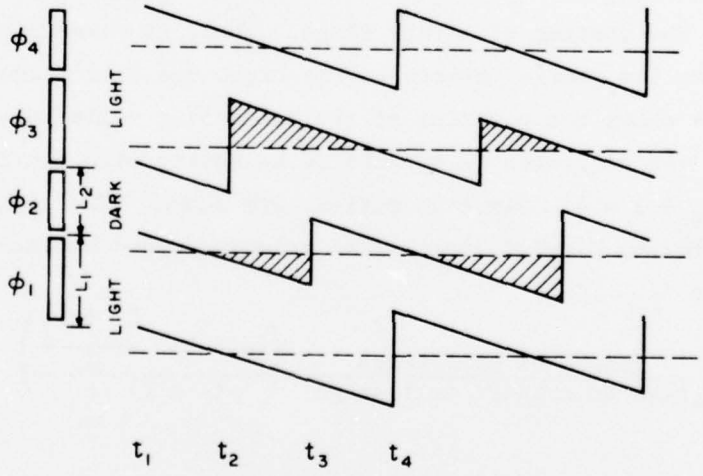


Figure 4. Position of the collection wells of the TDI array with four-phase electrode-per-bit clocking relative to the moving image in the form of light and dark bar pattern.

where Δt is the time between clock transitions, i.e., $f_{clock} = \frac{1}{(p+1)\,\Delta t}$. The shaded areas indicate the regions where the collecting well centered on the dark part of the image extends into the light regions.

The area of the larger triangular shaded region is $\frac{1}{2}\left(\frac{L_1}{2}\right)\left(\frac{L_1}{2}\right)\left(\frac{2p\Delta t}{L_1 + L_2}\right)$. The smaller area is $\frac{1}{2}\left(\frac{L_2}{2}\right)\left(\frac{L_2}{2}\right)\left(\frac{2p\Delta t}{L_1 + L_2}\right)$. There is one of each such triangular area for every p time periods. Therefore, the fraction for dark in light is

$$\text{Fraction} = \frac{\frac{\Delta t p}{(L_1 + L_2)}\left[\frac{L_1^2}{4} + \frac{L_2^2}{4}\right]}{p\Delta t\,\frac{p+1}{p}\left(\frac{L_1 + L_2}{2}\right)}$$

$$= \left(\frac{p}{p+1}\right)\frac{(L_1^2 + L_2^2)}{(L_1 + L_2)^2}\left(\frac{1}{2}\right)$$

The contrast is reduced by twice this amount since the light wells spend an equal time in the dark, so that

$$CTF = 1 - \left(\frac{p}{p+1}\right)\frac{(L_1^2 + L_2^2)}{(L_1 + L_2)^2}$$

In this case the resolution center-to-center spacing is given by:

$$D = \left(\frac{p+1}{p}\right)\frac{(L_1 + L_2)}{2}$$

An example of such a structure would be $L_1 = 0.4$ mil, $L_2 = 0.3$ mil and $p + 1 = 4$. Here the resolution center-to-center would be 0.470 mil and the CTF at the Nyquist limit would be 0.61735. If all the gates were 0.4 mil, the center-to-center spacing would increase to 0.533 mil and the CTF would increase only slightly to 0.62500. Therefore, using $L_2 = 0.3$ mil vs 0.4 mil would provide a 10% decrease in chip size at a negligible change in CTF.

2. CTF for Three-Phase Clocking

This discussion assumes a standard three-phase clocking scheme but with unequal gate lengths, L_1, L_2 and L_3. Using an analysis similar to the ripple-clocking case, the CTF can be shown to be:

$$CTF = 1 - \frac{11(L_1^2 + L_2^2 + L_3^2) - 2(L_1L_2 + L_1L_3 + L_2L_3)}{36(L_1 + L_2 + L_3)^2}$$

The resolution center-to-center spacing is:

$$D = L_1 + L_2 + L_3$$

An example is a three-phase device with L_1 = 0.3 mil, L_2 = 0.2, and L_3 = 0.2. Here the resolution center-to-center is 0.7 mil and the CTF is 0.91213. If the gates were all equal to 0.3 mil, the resolution center-to-center would be 0.9 mil and the CTF 0.91667.

Finally, Fig. 5 summarizes the CTF rolloff for various configurations. Generally the electrode-per-bit clocking approach results in smaller PEL dimensions and correspondingly higher Nyquist limits but more CTF rolloff. The three-phase approach has better CTF characteristics but larger dimensions.

D. SYSTEM/TECHNOLOGY TRADE-OFFS

In order to fabricate the high-speed page-reader for the lowest cost, it is desirable to make these devices on the smallest area of silicon, provided this does not lead to very expensive device processing. A reasonable measure of process complexity is how many mask levels are used in the process. This, however, does not consider whether or not some processing steps may be more critical than others. Therefore, qualitative comparisons of the relative process complexities are rather difficult. However, the relative cost of devices made by similar processes that are expected to give comparable yields can be estimated on the basis of the required areas of silicon. In this section the silicon areas required for Systems A, B, C, and D, shown in Fig. 1, are estimated for different CCD technology implementations. These results are summarized in Table 1.

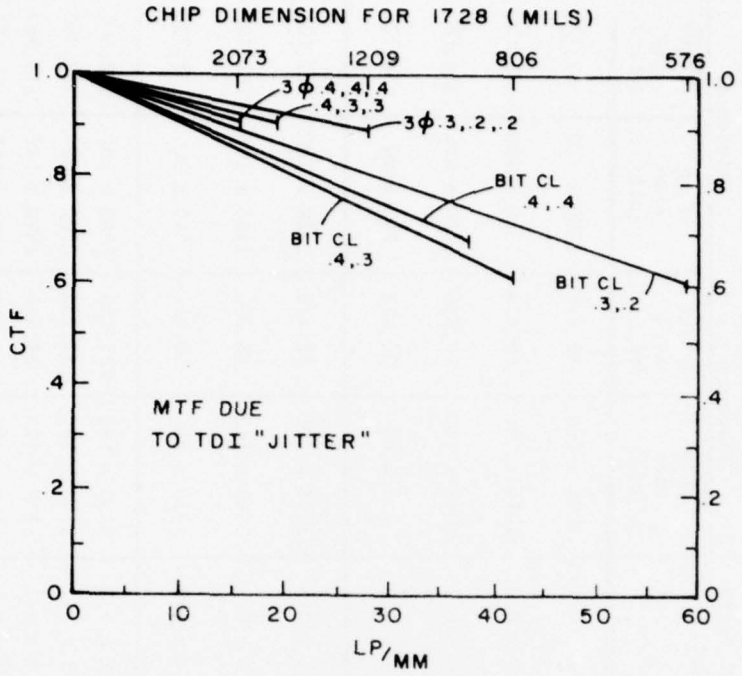


Figure 5. Contrast modulation function due to the TDI jitter for TDI array with:

- o Three-phase clock and 0.4, 0.4, 0.4; 0.4, 0.3, 0.3; and 0.3, 0.2, 0.2-mil gates.
- o Four-phase electrode-per-bit (BIT CL) with 0.4, 0.4; 0.4, 0.3; and 0.3, 0.2-mil gates.

In the column "CCD Technologies" in Table 1, 2-poly refers to the standard two-phase CCDs; 2 + 1 poly refers to standard two-phase CCD in the TDI array with additional level of polysilicon for the transfer gates between the multiplexed output registers; 3-poly refers to triple polysilicon CCDs used either only for the TDI array, or for both the TDI and the output register, as in the case of Systems C and D; and 1-poly refers to single polysilicon CCDs.

The second column of Table 1 describes the clocking for the TDI array. Here, we are considering the four-phase electrode-per-bit clock, when applicable. In the case of Systems C and D the electrode-per-bit clock offers no advantage as the picture element (PEL) size is determined by the stage length of the output register. The electrode-per-bit clock also can not be used with a normal three-phase CCD.

TABLE 1. GENERAL SPECIFICATIONS FOR 1728x96 AND 2200x96 ELEMENT TDI-CCD PAGE READERS

	CCD TECHNOLOGY	TDI CLOCK	PEL SIZE (mil)	1728 Horizontal Elements		2200 Horizontal Elements	
				chip size (mil)	active area (mil^2)	chip size (mil)	active area (mil^2)
SYSTEM A	(a) 2-poly	4-phase ripple clock	0.6 x 0.6	1096 x 100	68,428	1380 x 100	87,120
	(b) 2-poly TDI 2-1 poly output	4-phase ripple clock	0.6 x 0.6	1096 x 100	68,428	1380 x 100	87,120
	(c) 3-poly TDI 2-1 poly output	3-phase	0.6 x 0.7	1096 x 100	78,736	1380 x 100	104,880
	(d) Offset gate	4-phase ripple clock	0.4 x 0.4	750 x 80	30,412	940 x 80	38,720
SYSTEM B	(a) 2-poly TDI 2-1 poly output	4-phase ripple clock	0.6 x 0.6	1096 x 100	68,428	1380 x 100	87,120
	(b) 3-poly TDI 2-1 poly output	3-phase	0.6 x 0.7	1096 x 100	78,736	1380 x 100	104,880
	(c) Offset gate	4-phase ripple clock	0.4 x 0.4	750 x 80	30,412	940 x 80	38,720
SYSTEM C or D	(a) 1-poly	3-phase	1.2 x 1.2	2133 x 180	257,052	2700 x 180	327,360
	(b) 2-poly	2-phase	1.2 x 1.2	2133 x 180	257,052	2700 x 180	327,360
	(c) 3-poly	3-phase	0.7 x 0.7	1260 x 120	89,466	1600 x 120	113,960
	(d) Offset gate	2-phase	0.6 x 0.6	1116 x 110	66,355	1380 x 110	84,480

The chip sizes for the 1728- and 2200-element sensors represent only a rough estimate. The active area for these two devices include only the photosensitive area of the TDI and a rough estimate of the additional area needed for the output register.

Inspection of Table 1 points out that from the silicon area point of view, the most attractive approach is System A or System B, using the offset-gate CCDs. The active areas of these devices of 30,412 and 38,720 sq. mil for the 1728- and 2200-element sensors, respectively, are not very much larger than the double polysilicon 16 K RAM's under development in a number of companies. The feasibility of this device, however, depends on the practicality of the offset-gate CCD with 0.6-mil long stages. The other extreme choice is the System C or System D using single polysilicon CCDs. The active areas of these devices are comparable to the commercially available RCA 512x320 CCD area image sensor, the Big Sid (silicon-imaging device).

SECTION III

PAGE-READER TEST CHIP

A. CCD TECHNOLOGY AND CHIP DESIGN CONSIDERATIONS

The system/technology trade-off analysis in Section II.D concluded that the most attractive approach for the full-size page reader is to use System A or System B with the offset-gate CCD structure. However, when this analysis was done, a buried-channel version of the offset-gate CCDs was not available at RCA Laboratories. Therefore, a decision was made in agreement with NOSC to postpone for about three months the final design of the page-reader test chip to try out our ideas for fabricating buried-channel offset-gate CCDs. Since this was carried out only with RCA funds, we will not describe here the details of this work. The conclusion of this work, however, was that after two processing runs we did not achieve buried-channel CCDs operating with low transfer losses without fat zero. Therefore, at that point, because of the time limitation, it was decided not to wait for further results on the offset-gate devices, but to go ahead with the design of the page-reader test chip based on the two-level polysilicon buried-channel CCD technology previously developed at RCA Laboratories.

A 748x96-element TDI-CCD line sensor with 4:1 multiplexed output was chosen as the main device for the page-reader test chip. This 748x96-element array represents about 35% of the area of the 2200x96-element TDI line sensor, and it contains all of the features necessary for construction of the full-size page reader.

The 748x96-element page-reader test chip was designed for processing with the two-level polysilicon CCD technology modified to assure high large-area yield and with reduced feature size to obtain an effective resolution in the TDI array of 0.6x0.6 mil PELs. To achieve this resolution, the TDI gates were designed with 0.35-mil gates and 0.1-mil spaces for both levels of polysilicon. This results in 0.35 storage gates and 0.1-mil transfer barriers. The resulting 0.45-mil electrodes in conjunction with 4-phase electrode-per-bit clocked TDI array results in an effective vertical PEL dimension of 0.6 mil. The horizontal PEL dimension of 0.6 mil has been defined by 0.4-mil TDI-CCD channels and 0.2-mil channel stops.

The block diagram of the 748x96-element page-reader test chip is shown in Fig. 6. As is shown in this figure, the 748x96-element TDI array, in addition to the 4:1 multiplexed output registers can also be read out by a double 2:1 multiplexed output register. The main structural difference between the two types of 4:1 multiplexed outputs is that in the case of 4:1 multiplexed output (shown on the bottom) the output registers have 2.4-mil long CCD stages, while in the case of the double 2:1 multiplexed output the output registers have 1.2-mil long stages. The advantage of the 4:1 multiplexed output registers with 2.4-mil stages is that they can be laid out with two-level polysilicon gates using rather noncritical design rules. The layout of 2:1 multiplexed output registers with 12-mil stages, on the other hand, requires much tighter design rules.

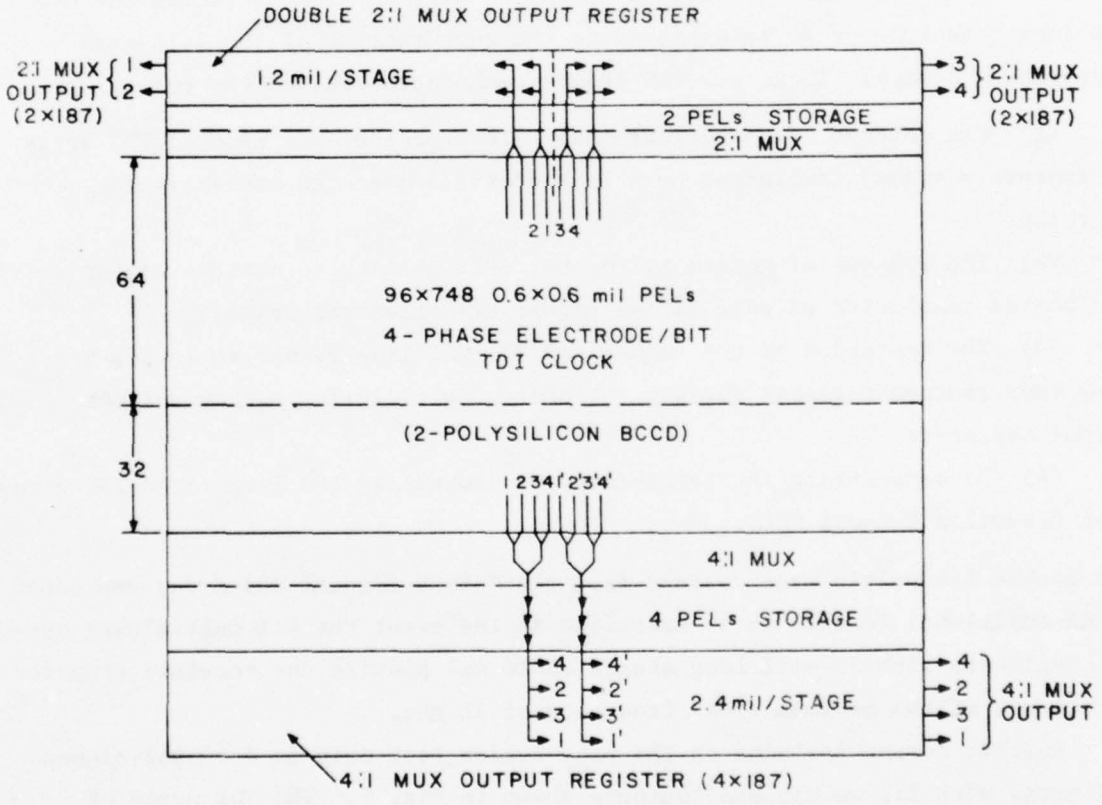


Figure 6. Block diagram of 748x96-element TDI-CCD line sensor with four-phase electrode-per-bit clocking array/two types of 4:1 multiplexed output.

The 4:1 multiplexed output registers were designed with minimum line width of 0.3 mil and spacing of 0.1 mil on the first-level polysilicon and minimum line width of 0.3 mil, and spacing of 0.2 mil on the second-level polysilicon. The 2.4-mil stages of these registers were laid out with the active gate length of 0.6 mil for both levels of polysilicon and 0.2-mil gate overlap.

The double 2:1 multiplexed output registers with 1.2-mil stages were laid-out with 0.1-mil gate overlaps. The minimum dimensions of the first-level polysilicon in these registers outside of the CCD channels correspond to 0.2-mil lines and 0.1-mil spaces, and for the second-level polysilicon correspond to 0.2-mil lines and 0.15-mil spaces.

The general strategy in designing the page-reader test chip was to optimize the layout of the 4:1 multiplexed readout of the 748x96-element TDI array. This device was intended to be the vehicle for demonstrating the new CCD imager techniques to be employed in the construction of the full-size page-reader device. These new CCD imager techniques include the following:

(1) The concept of using four-phase electrode-per-bit clocked TDI array to improve vertical resolution by a factor of 1.5 over the conventional approach.

(2) The concept of horizontal output multiplexing to achieve higher horizontal resolution as well as the higher effective scan rate.

(3) The operation of the high-speed TDI-CCD line sensor employing a temporary storage register between the charge multiplexing switch and the output registers.

(4) To demonstrate the feasibility of processing the large-area TDI array with 0.6-mil x 0.6-mil PELs.

The double 2:1 multiplexed readout from the 748x96-element TDI array was added as an additional feature to be exercised in the event the 4:1 multiplexed output registers with 2.4-mil long stages could not provide the required transfer effeciency at the maximum clock frequency of 21 MHz.

Another device included on the page-reader test chip is a 540x32-element TDI array with 2:1 multiplexed outputs shown in Fig. 7. The TDI array of this device is in the form of three-level polysilicon three-phase CCDs with 0.7-mil x 0.7-mil PELs. The 0.7 mil per stage three-phase CCD is constructed

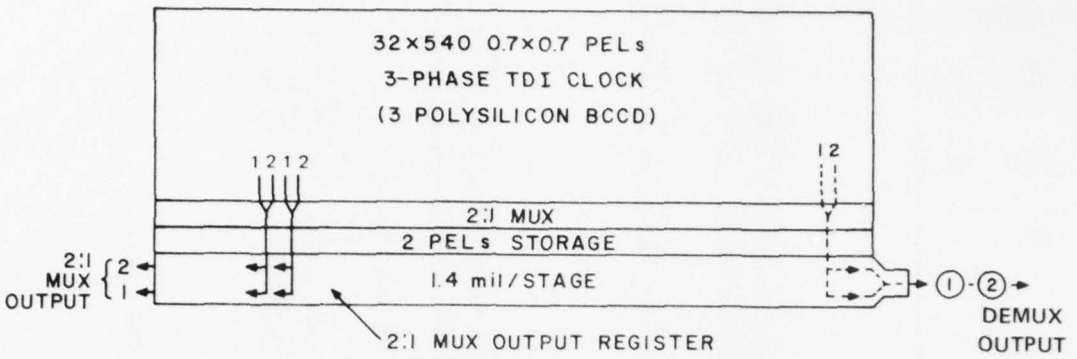


Figure 7. Block diagram of 540x32-element, three-phase TDI with 2:1 multiplexed output.

with 0.3-mil gate for the first-level polysilicon and nominal gate length of 0.2 mil for the second and third-level of polysilicon. This three-level polysilicon has a 0.3-mil gate spacing for the second-level polysilicon and a 0.4-mil spacing for the first-level polysilicon. This structure was included on the page-reader test chip in case difficulty is encountered in processing the 748x96-element device with 0.1-mil gate spaces. As shown in Fig. 7 the 540x32-element array can be read out by the 2:1 multiplexed output registers in two ways. One way is to use two parallel outputs shown on the left side of the array. The other available readout combines the signals from the two output registers into a single output, shown on the right side of the array.

B. PAGE-READER TEST CHIP LAYOUT

The size of the page-reader test chip is 582x232 mil. In addition to the 748x96-element double-polysilicon TDI array and the 540x32-element triple-polysilicon TDI array, the chip contains test structures of the 2:1 and 4:1 charge multiplexer, output amplifier test structures, and other test devices for process control. The metallization level of the page reader test chip is shown in Fig. 8 to illustrate the overall chip layout.

The large number of metal lines connecting the two sides of the 748x96-element include the connections to the gates of the TDI arrays. As has been shown previously in Fig. 6, this TDI array is connected with two sets of gates.

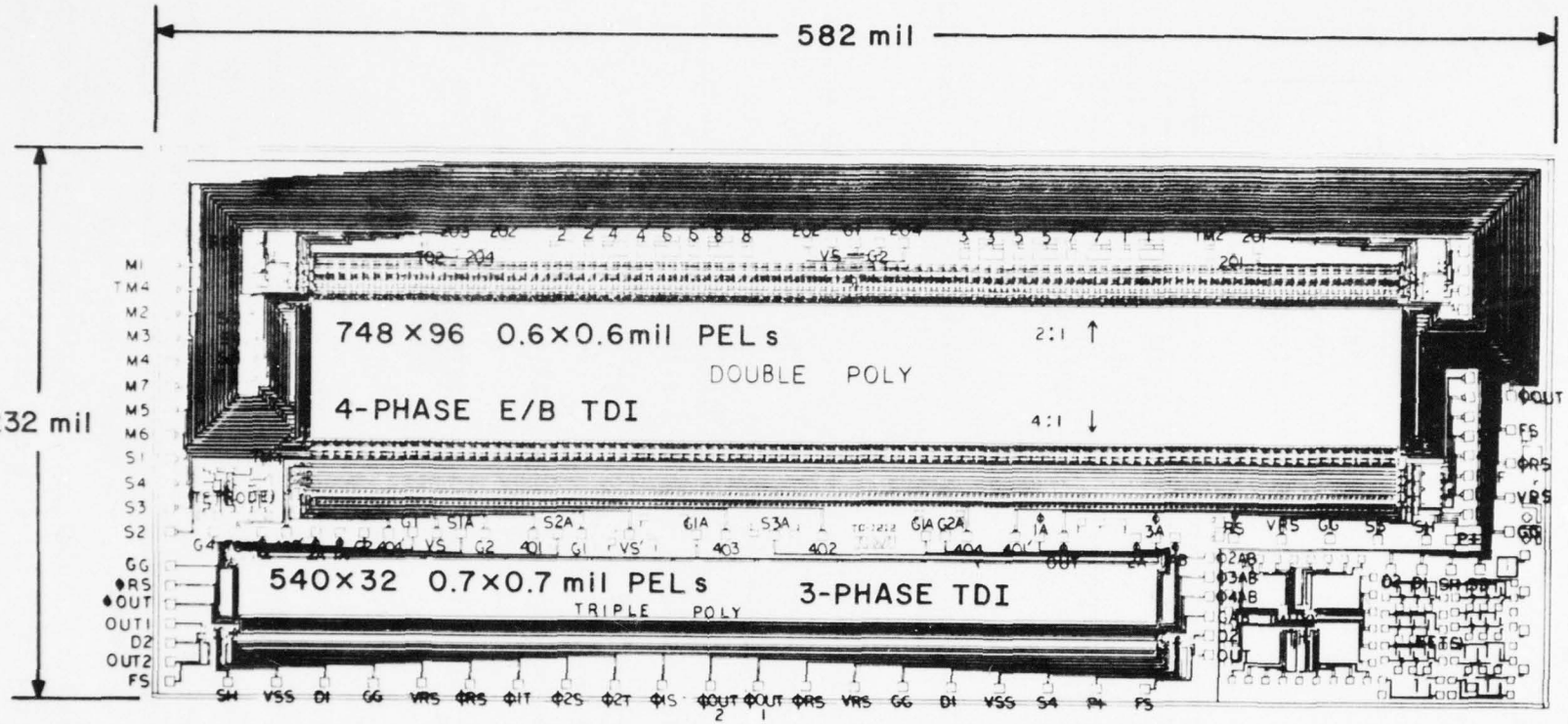


Figure 8. Metallization level of the page-reader test chip.

One set corresponds to 32 TDI elements, and the other set to 64 TDI elements. A separate 32-element TDI array has been included to provide a device for NOSC with a smaller number of TDI elements, and also to determine whether higher processing yield can be achieved with the smaller area device.

The layout of the page-reader test chip is illustrated in more detail by the photomicrographs of the sections of the 748x96-element array shown in Figs. 9 through 14, respectively. Figure 9 shows a photomicrograph of the whole chip where five sections have been indicated. These five sections are shown in Figs. 10 through 14. Figure 10 shows the electrical input section of the 4:1 multiplexed array and the output section of this array is shown in Fig. 11. Figures 12 to 14 show the 2:1 multiplexed structure. Figure 12 shows the output section on the left side. Figure 13 shows the center section. This section has an input to the reference channel and the separation between the right and left side output registers can be seen. Figure 14 shows the output section on the right side. As may be seen in the above figures, the TDI gates of these two arrays have been connected from both sides of the array to provide redundancy for electrical connections to these gates, and also to reduce the RC delay time of the TDI clocks by a factor of four. In addition all the gates which require faster charge transfer from the TDI gates have been designed with metal straps. This includes the gates involved in the 2:1 and 4:1 charge multiplexing, the four-PEL temporary storage register, and the gates controlling the interregister charge transfers in the output registers. The construction and operation of the 748x96-element array is described more fully in the following section.

C. CONSTRUCTION AND OPERATION OF 748x96-ELEMENT TDI-CCD LINE SENSOR

1. General Description of the Device

In this section a more complete description will be given of the construction and the operation of the 4:1 multiplexed output of this TDI array. A schematic sketch of the complete 748x96-element TDI array with 4:1 multiplexed output is shown in Fig. 15. The second-level polysilicon gates are illustrated in this figure by solid lines. The first-level polysilicon gates are shown as dotted lines. In the actual layout the second-level polysilicon gates overlap the first-level polysilicon gates. For simplicity, the first-level

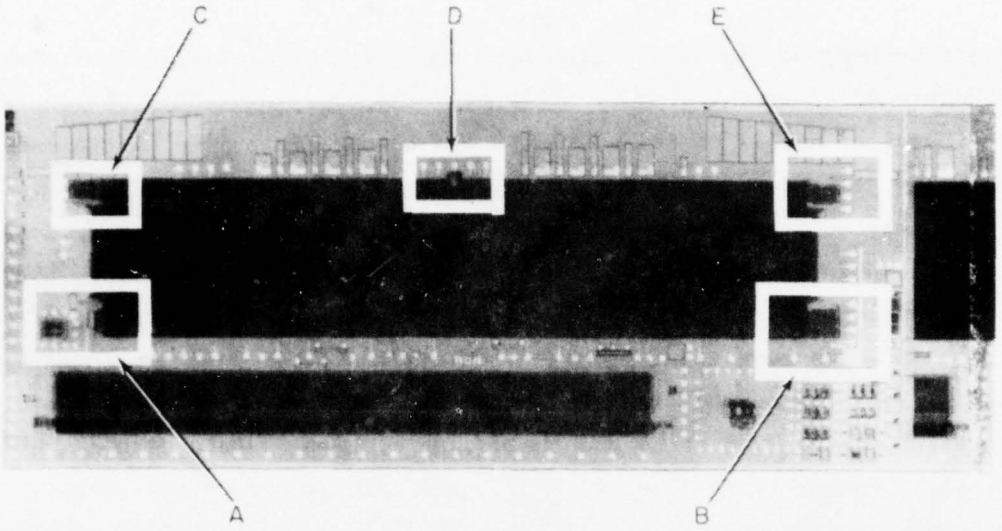


Figure 9. Photomicrograph of the 748x96-element page-reader test chip.

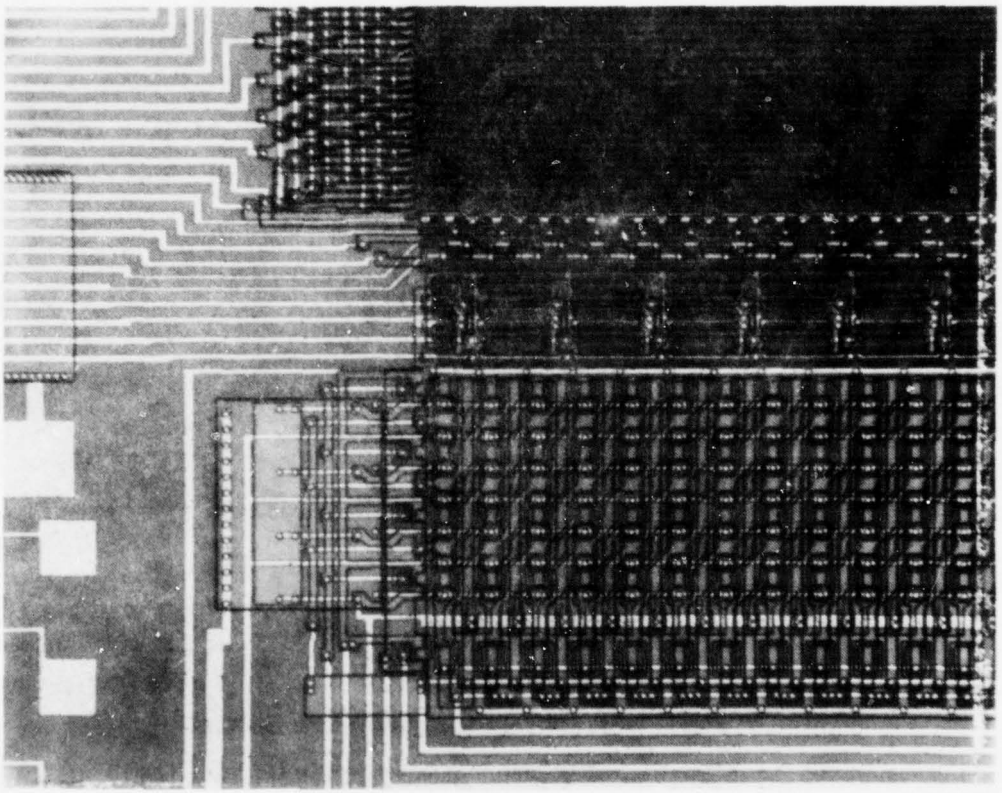


Figure 10. The input part of the 4:1 multiplexed output registers shown in Section A in Figure 9.

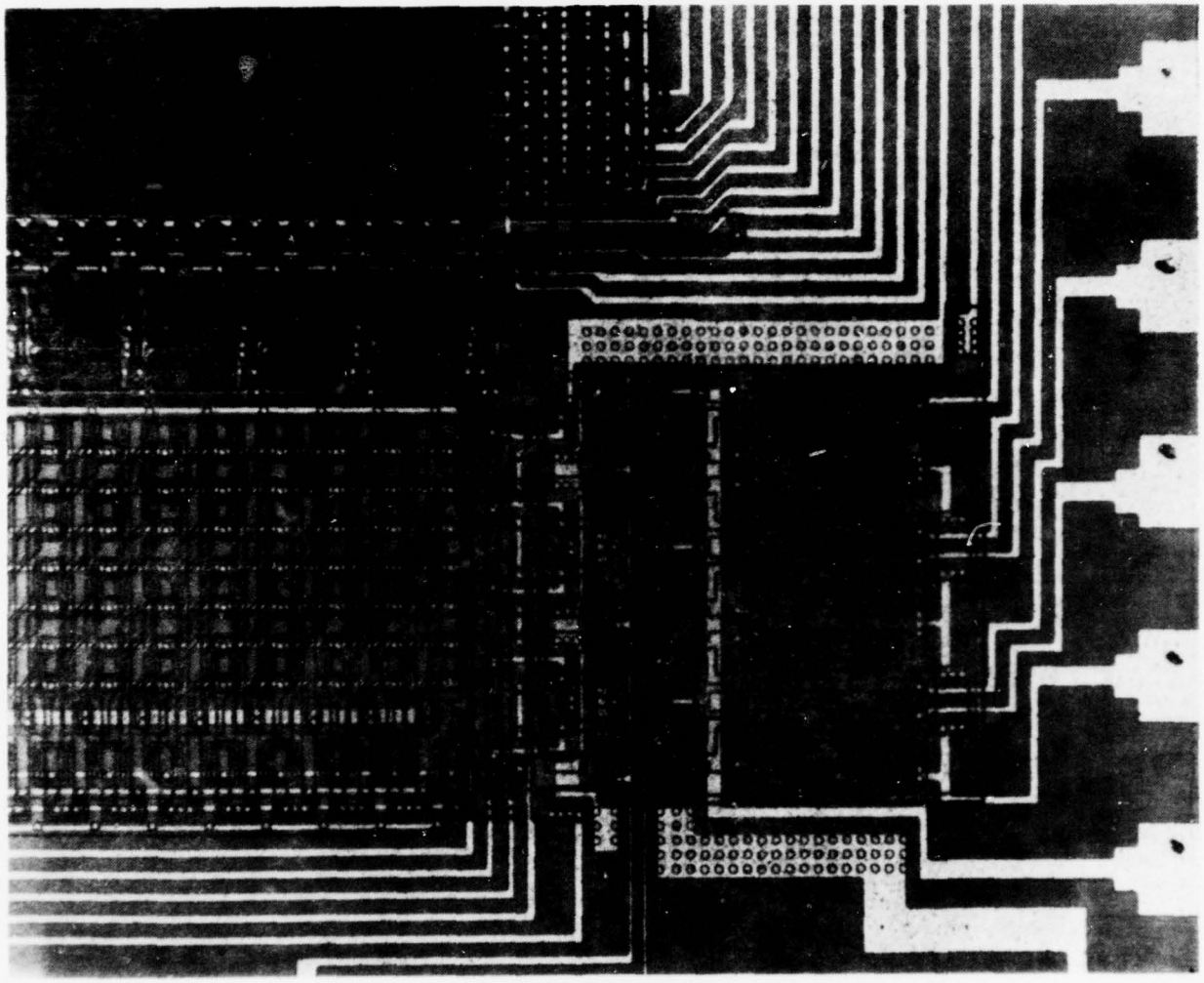


Figure 11. The output part of the 4:1 multiplexed output registers as shown in Section E, Fig. 9.

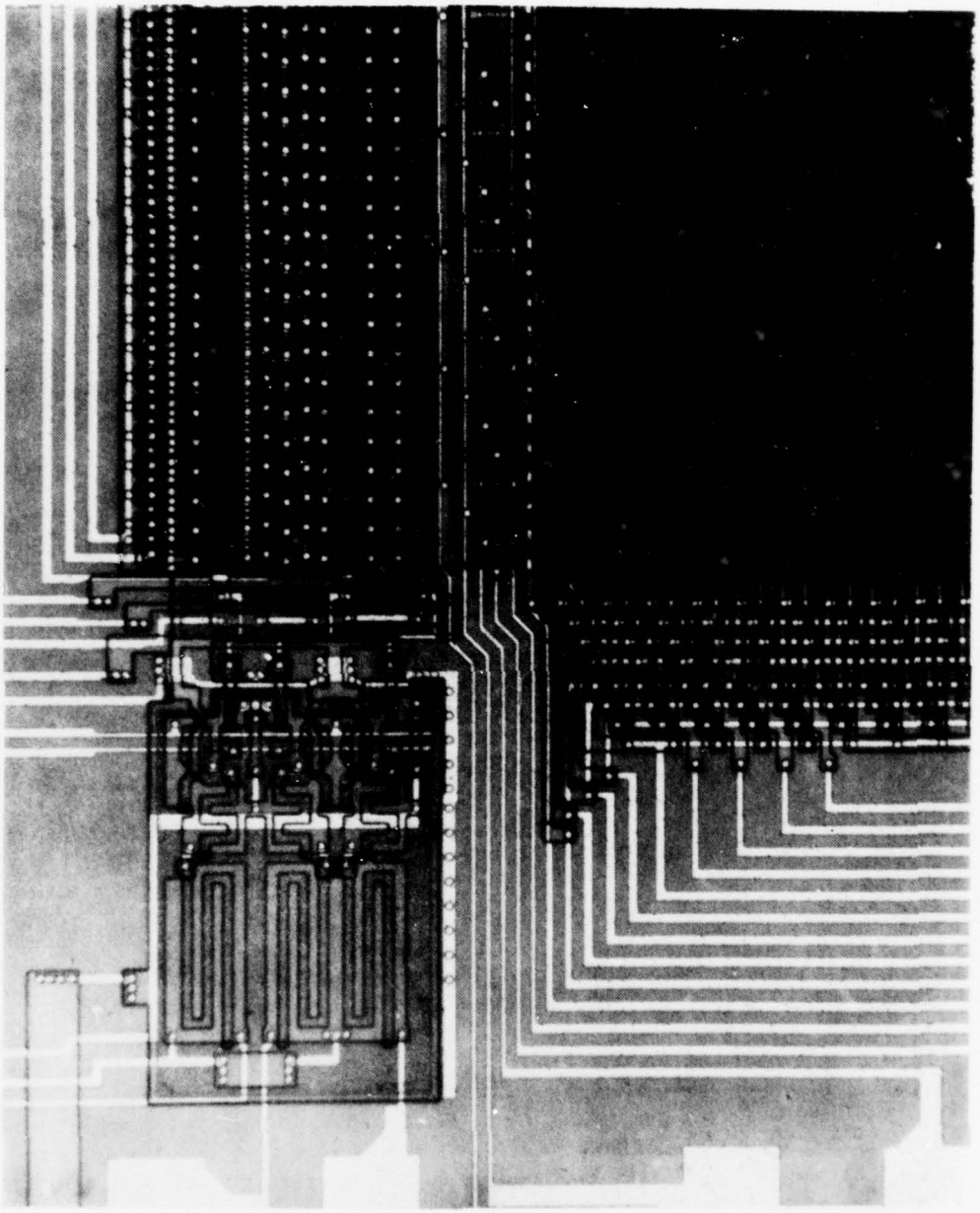


Figure 12. The left-hand output of the double 2:1 multiplexed output registers (shown in Section C, Fig. 9).

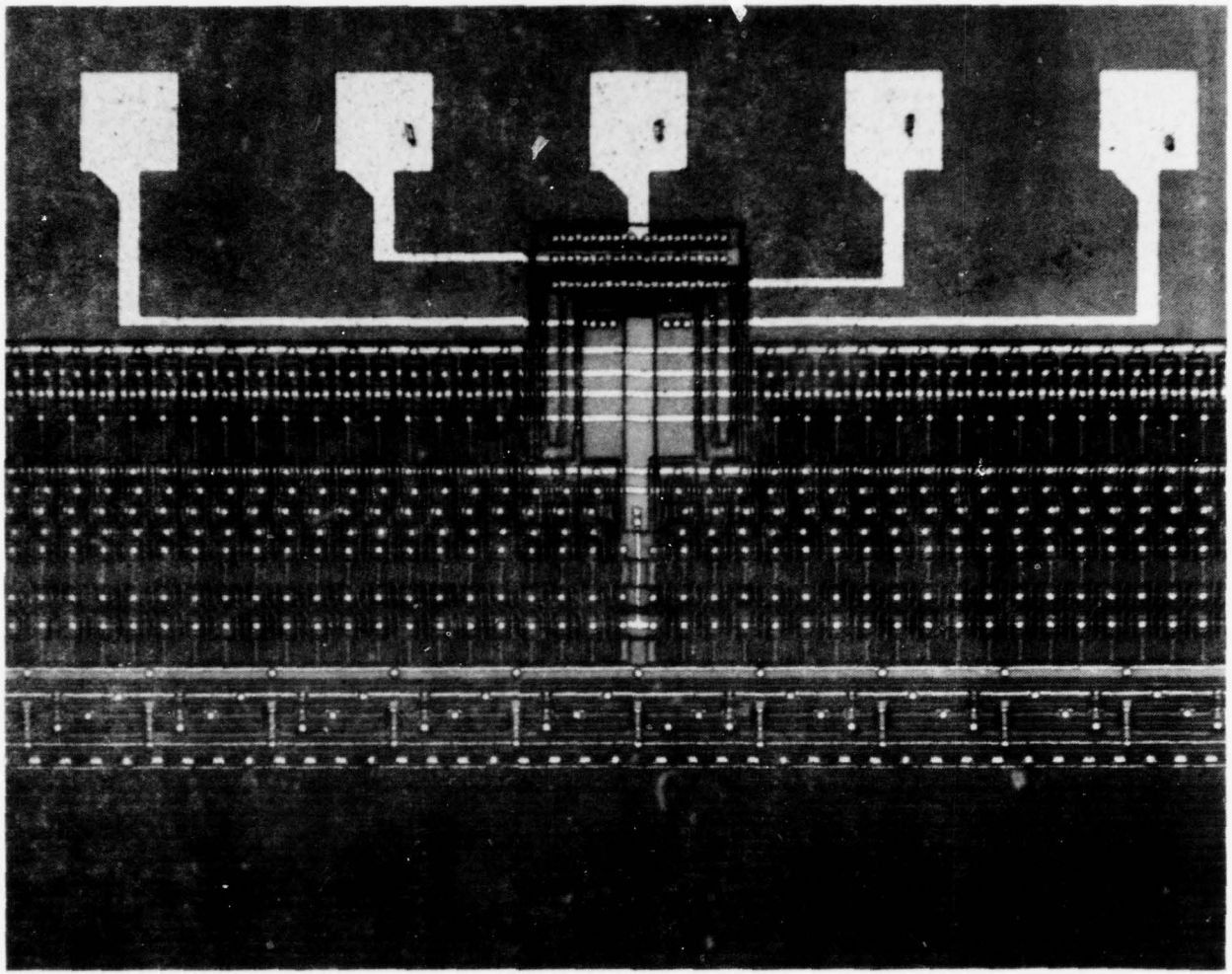


Figure 13. The middle part of the double 2:1 multiplexed output registers (shown in Section D, Fig. 9). The array detail illustrated in this figure shows the electrical inputs to the two reference registers.

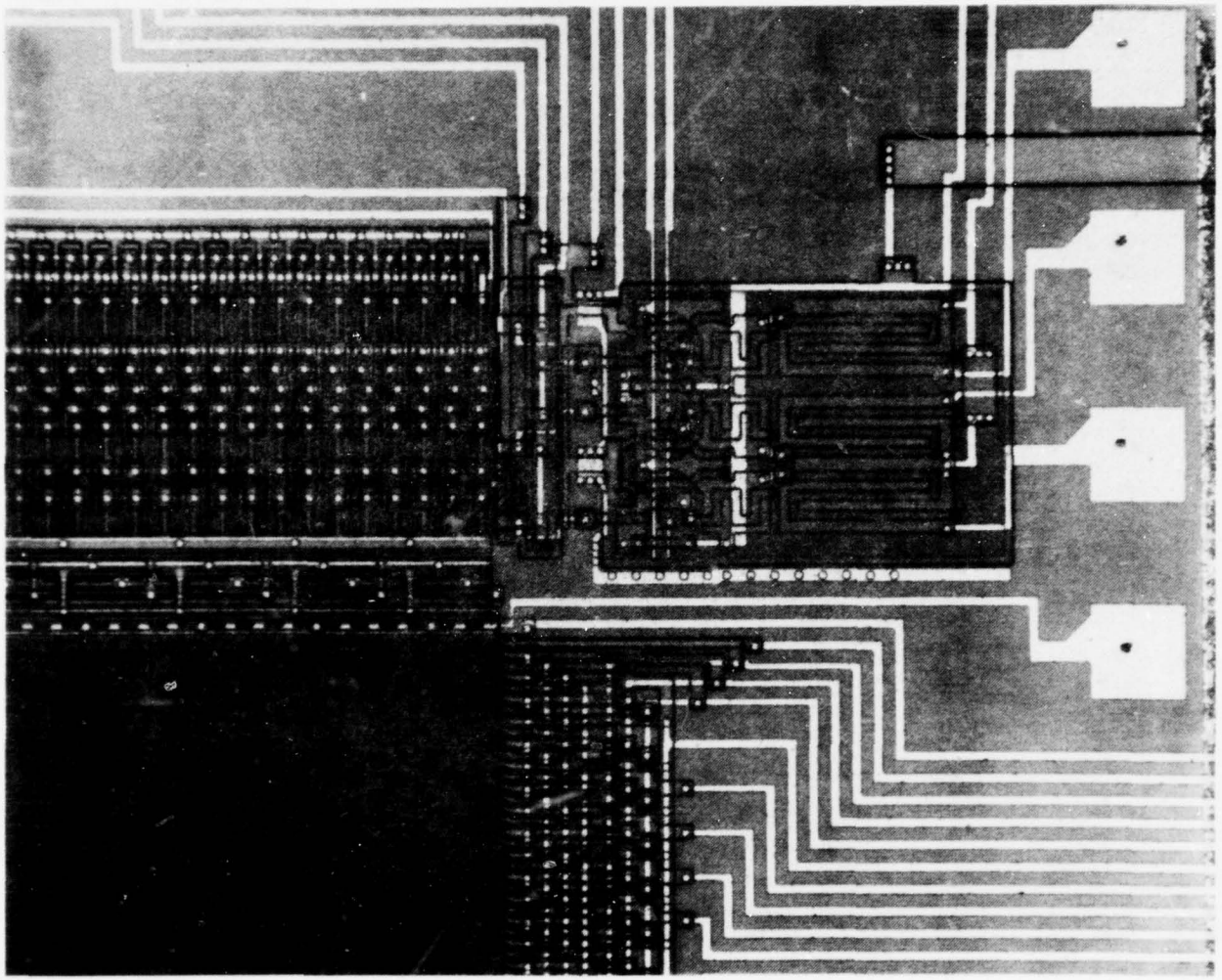


Figure 14. The right-hand part of the double 2:1 multiplexed output registers (shown in Section E, Fig. 9(e)).

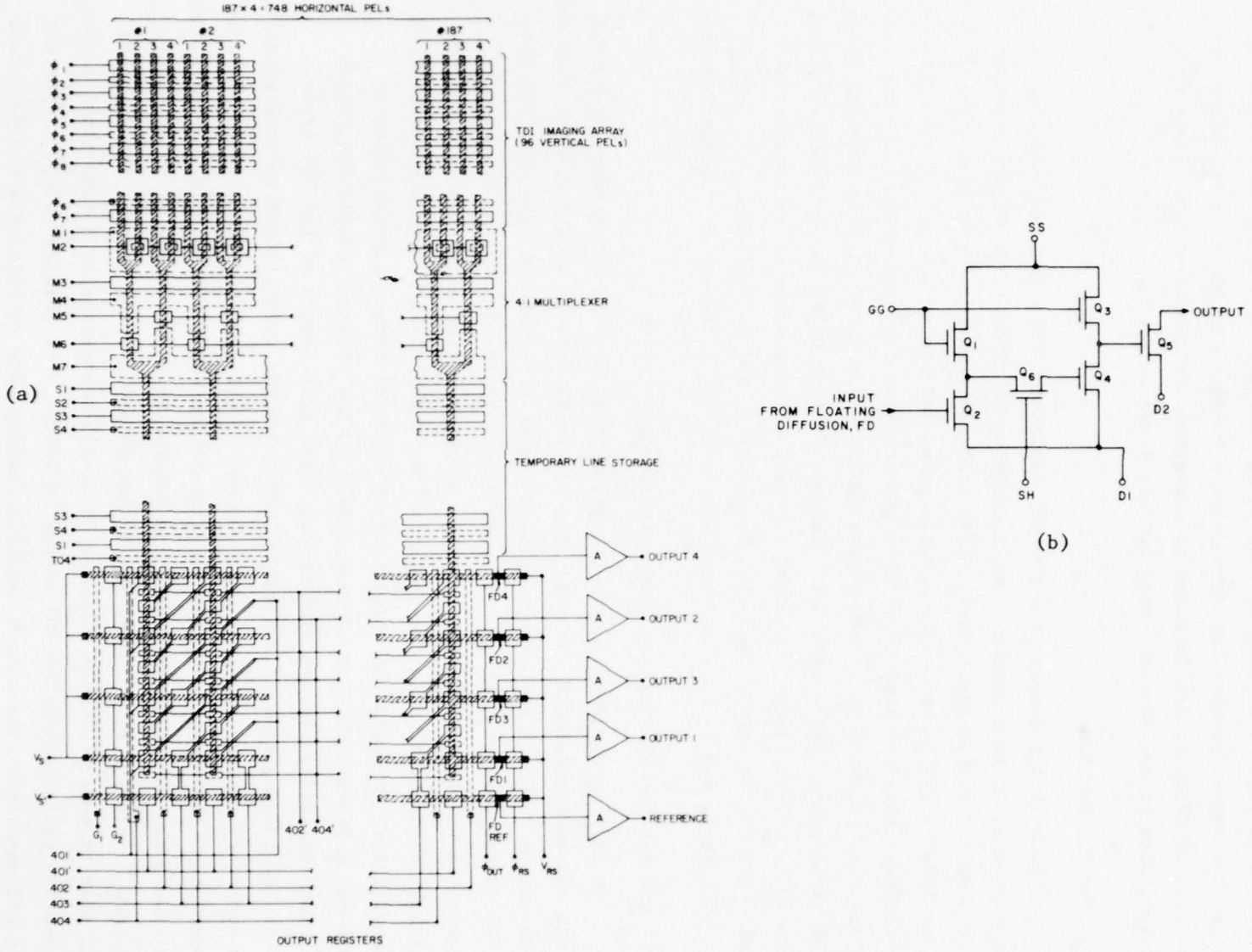


Figure 15. (a) Schematic layout of the 748x96-element array with four-phase electrode-per-bit clocked TDI array and 4:1 multiplexed output. (b) Three-stage source follower output amplifier.

polysilicon gates are shown in Fig. 15 as narrower than the actual size. In fact, the spaces between the second-level polysilicon gates in the direction of the CCD channels are intended to represent the length of the first-level polysilicon gates, however, they are not drawn to scale.

2. The TDI Section

Figure 15 illustrates how the 748 horizontal PELs are subdivided into four groups, or four frames, each containing 187 PELs. The 96 TDI elements are composed of 124 electrodes, where each electrode corresponds to two gates (the first polysilicon is the storage gate, and the second polysilicon gate is a transfer gate). Since this TDI array has been designed to operate on a four-phase electrode-per-bit clock scheme it has three vertical PELs for every four TDI electrodes. Since each TDI electrode is made up of two polysilicon gates, the TDI array is clocked by eight separate clocks, shown as ϕ_1 to ϕ_8. In operation of the array, the pairs of clocks ϕ_1 and ϕ_2, ϕ_3 and ϕ_4, ϕ_5 and ϕ_6, as well as ϕ_7 and ϕ_8 have the same waveforms but different dc voltage levels.

3. The 4:1 Multiplexer and Temporary Storage Section

In this multiplexer section, every fourth vertical CCD channel is routed into one horizontal CCD channel. The clocks M1 through M7 are used to provide the timing to clock the charge through the multiplexer. A more detailed description of how this charge multiplexing, or charge gating, is achieved is described below. It should, however, be mentioned here that the new charge gating technique used in the design allows a layout with very high horizontal resolution. In fact, the resolution of this TDI array, corresponding to 0.6-mil x 0.6-mil PELs is limited mainly by the vertical resolution, which in turn is limited by the minimum practical gate length of the TDI array.

The loading time of the output registers can be minimized by incorporating a temporary storage register which holds four of the PELs from the multiplexer section. The temporary storage section of the array corresponds to four stages of two-phase CCD registers which are powered by clock phases S1 to S4. Here, S1 and S3 are transfer gates, and S2 and S4 are storage gates. The function of this temporary storage register is to allow essentially a full line readout time for multiplexing the TDI output by loading the parallel output registers in minimum time. The output register loading time in this design should take

about 2.0 μs, or less than 10% of the minimum line readout time. To insure the minimum time for the loading of the output registers, all of the gates involved in this type of transfer have been strapped by aluminum busses.

The temporary storage register is separated from the output register by a transfer gate, TO4. This gate is first-level polysilicon to obtain better charge transfer characteristics into the output register.

4. The Output Register Section

The construction of the output registers is shown in Fig. 15. Although this is a schematic representation, it illustrates the general strategy used for the layout of the output registers. There are actually five parallel output registers. Each of these registers has 187 two-phase stages, on electrical input, and an output amplifier. The first four output registers serially read out the 4:1 multiplexed output of the TDI array. The fifth output register has been included in this design to serve as a reference channel for differentially canceling the clock pickup in the outputs.

The two-phase clocks for the operation of the output registers consist of clock phases 401, 401', 402, 403, and 404; where the clocks 401, 401', and 403 drive the transfer gates and the clocks 402, and 404 drive the storage gates. Other gates and timing clocks for the output register are the input gates, G_1 and G_2. The last gate before the floating diffusion, FD, is ϕ_{OUT}. The gate resetting the floating diffusion to the drain potential V_{RS} is ϕ_{RS}. The voltage V_S is the voltage driving the source diffusions of the first four output registers. The fifth, the reference register, has a separately controllable source diffusion voltage, V'_S, so that an independent charge signal can be introduced into the reference register during the readout of the TDI array by the first four registers. In this case, the four output registers will be operated without the electrical input.

The floating diffusion, FD, output of each channel is amplified by a three-stage MOS amplifier, to provide maximum dynamic range and frequency response up to the clock frequency of 21 MHz. The first two stages are designed to operate as source followers. They are operated by a sample-and-hold switch in the form of the MOS device, Q6, which is controlled by the sample-and-hold pulse, SH. In addition to the externally adjustable dc voltages, D1, D2 and SS, the output amplifier has a common gate voltage control, GG, to adjust

the operation of the source follower load devices Q_1 and Q_3. The main purpose of the second source follower stage, Q_3 and Q_4 is to isolate the sample-and-hold device, Q_6, from the high-capacitance output device Q_5.

The data transfer from the temporary storage section into the output registers is described in the following. In this charge transfer the four-stage temporary storage registers are clocked together with the four output registers in an interregister transfer mode. The contents of the temporary storage registers are transferred to the four output registers, by a two-phase interregister clocking scheme. The clocks involved in this transfer are S1 to S4, TO4, 401, 403, 402', and 404'. During this vertical transfer from the temporary storage section into the output registers, the clock phases 402 and 404 act as channel stops preventing the charge from flowing horizontally in the output registers. Conversely, during the horizontal readout time, the clock phases 402', 404' and TO4 act as channel stops, preventing charge flow in the vertical direction.

5. Operation of the 4:1 Multiplexer

The operation of the 4:1 signal charge multiplexer, is illustrated in Figs. 16 and 17. This parallel-to-serial signal-charge gating is accomplished by two sequential binary switches. The first charge switch is formed by gates M1 and M2 which separates the channels 1 and 3 from channels 2 and 4. The window gate shown in a top view of Fig. 15 is shown in cross-sectional view in Fig. 16. The cross-sectional structure in Fig. 16(a) applies only to channels 2 and 4. The first polysilicon gate, M1, over these two channels contains a window and the second polysilicon gate that covers this window can be used to control the channel potential in the window. The other channels (1 and 3) have a continuous gate M1 and the charge transfer in that case is conventional.

The ideal operation of the charge gate shown in Fig. 16(a) is illustrated by the potential profile in Fig. 16(b). In this case, when gate M2 forms a barrier (as is illustrated by the solid line in Fig. 16(b)), the signal charge will be prevented from being transferred into the potential well under gate M4. But, when gate M2 is turned on (as is illustrated by the dotted lines), the signal charge originally stored under the left-hand part of gate M1 will be completely transferred to the potential well under gate M4.

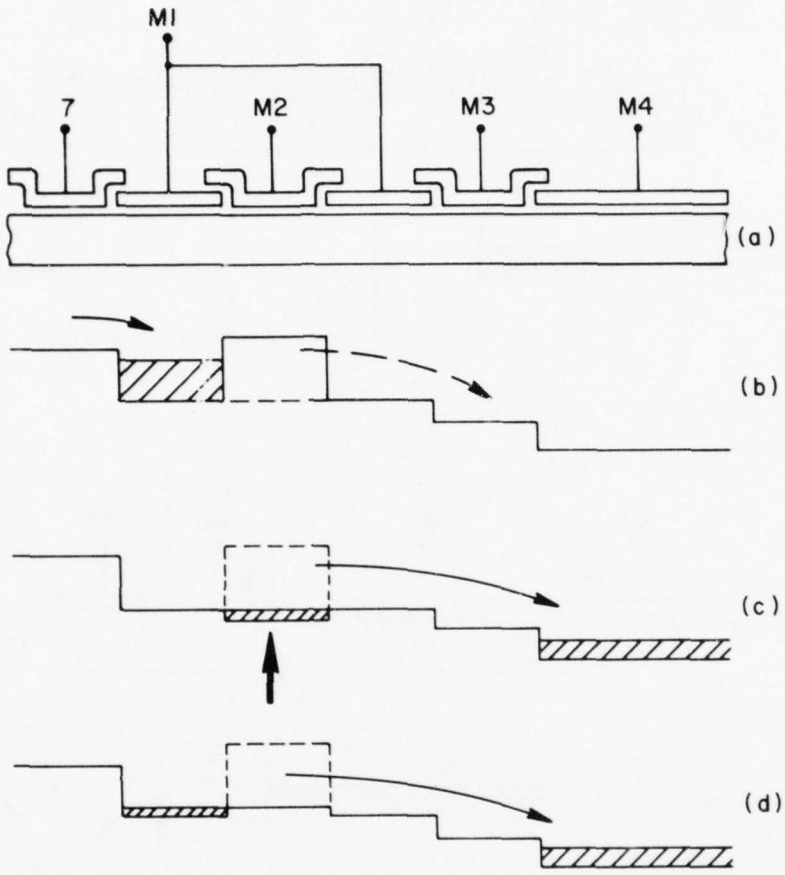


Figure 16. Construction schematic of the amplifiers used in the 748x96-element array, and operation in (b), (c), (d), of the "window-gate" charge switch used as the first 2:1 multiplexer in Fig. 15.

In actual operation, it is difficult to maintain the channel potential under gate M2 exactly equal to the channel potential under gate M1. Therefore, this charge gate must be operated in one of the modes shown in Fig. 16(c) or Fig. 16(d). Consider the mode illustrated in Fig. 16(c). During the transfer of the charge signal from the well under the left part of gate M1 a potential well is formed under gate M2. This well will momentarily trap some of the signal charge. However, it is possible to make a substantially complete charge transfer, if the fall time of the clock M2 is relatively slow. A slow fall time of M2 will assure that all the original charge under gate M2 is pushed

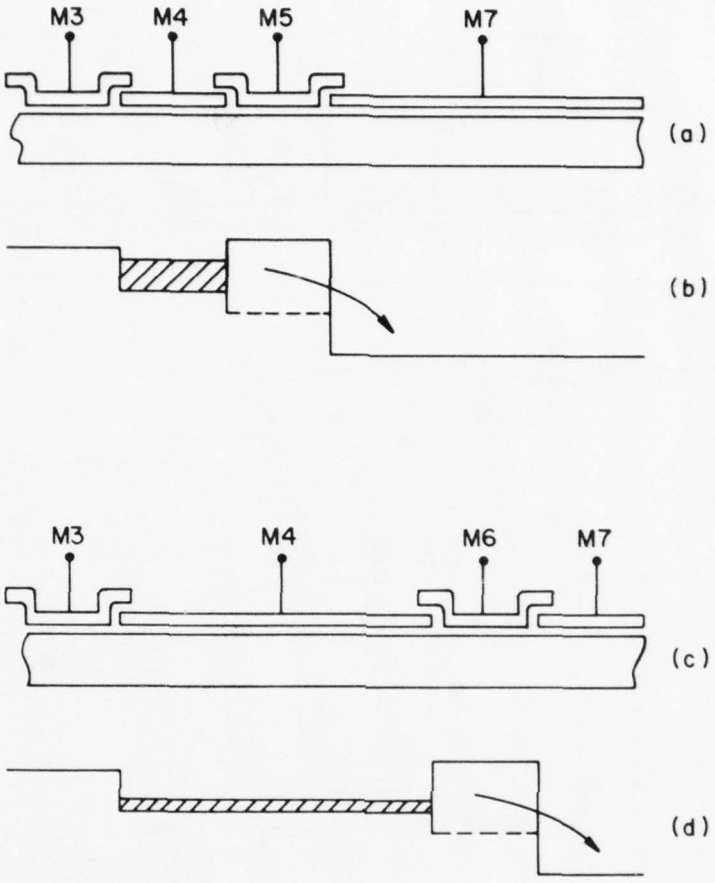


Figure 17. Construction in (a) and (c), and operation in (b) and (d) of the "interleaved gate" charge switch used as the second 2:1 multiplexer in Fig. 15.

from this well into the potential well under gate M4. Thus, no appreciable amount of charge can be trapped under the left-hand part of gate M1. However, any charge trapped at this position will tend to degrade the vertical MTF of the imager.

The second mode of operation of the charge gate is illustrated in Fig. 16(d). Here, during the transfer of charge to the potential well under gate M4, a potential barrier is formed under gate M2. Due to this potential barrier some charge will always be left behind under the left part of gate M1. This mode of transfer is referred to as incomplete transfer or a bucket-brigade mode of operation. In steady-state operation with a bias signal, or fat zero, a

typical transfer loss for this type of transfer is on the order of 10^{-3}. However, even without a fat zero, the expected charge transfer loss in this case is expected to be on the order of 10^{-2} (or 1%), which should have a negligible effect on the MTF of the TDI array.

The most important advantage of the first 2:1 multiplexing by the window gate is that it can be accomplished with very high resolution. The second charge switch is accomplished by the interleaved gates M4 and M7 which allow the charge to be transferred either by the transfer gate, M5, as is shown in Figs. 17(a) and (b), or by the transfer gate, M6, as is illustrated in Figs. 17(c) and (d). From the operational point of view, this second switch is much more straightforward, however, it does not allow the packing density that is possible with the window gate.

6. Calculated Performance of the Output Amplifier

The 748x96-element 4:1 multiplexed CCD page reader has four horizontal output data registers and one reference register. The signal is sensed by a floating diffusion and amplified by a three-stage source follower circuit as shown in Fig. 15(b). The first two source followers contain on-chip load transistors and a sample-and-hold transistor exists between the first and second stage. This circuit has been simulated with a computer analysis program (RCAP) and the transistor dimensions used in the analysis are shown in Table 2. The frequency response of this circuit is shown in Fig. 18. The 3 dB point is 21 MHz which is sufficient for the present application, since each channel must operate at 21 MHz to provide the 84-MHz data rate.

D. MASKS FOR 748x96 PAGE-READER TEST ARRAY

The masks for the test chip were photocomposed by means of an Electromask* laser-controlled machine, which has a specified step accuracy of 10 microinches. The overall chip dimension is 528 mil x 232 mil, and requires three reticles for the photocomposition. To maximize the yield, step-and-repeat master plates, rather than the normal working plates, were used for wafer processing.

*Electromask Corp., Woodland Hills, Calif.

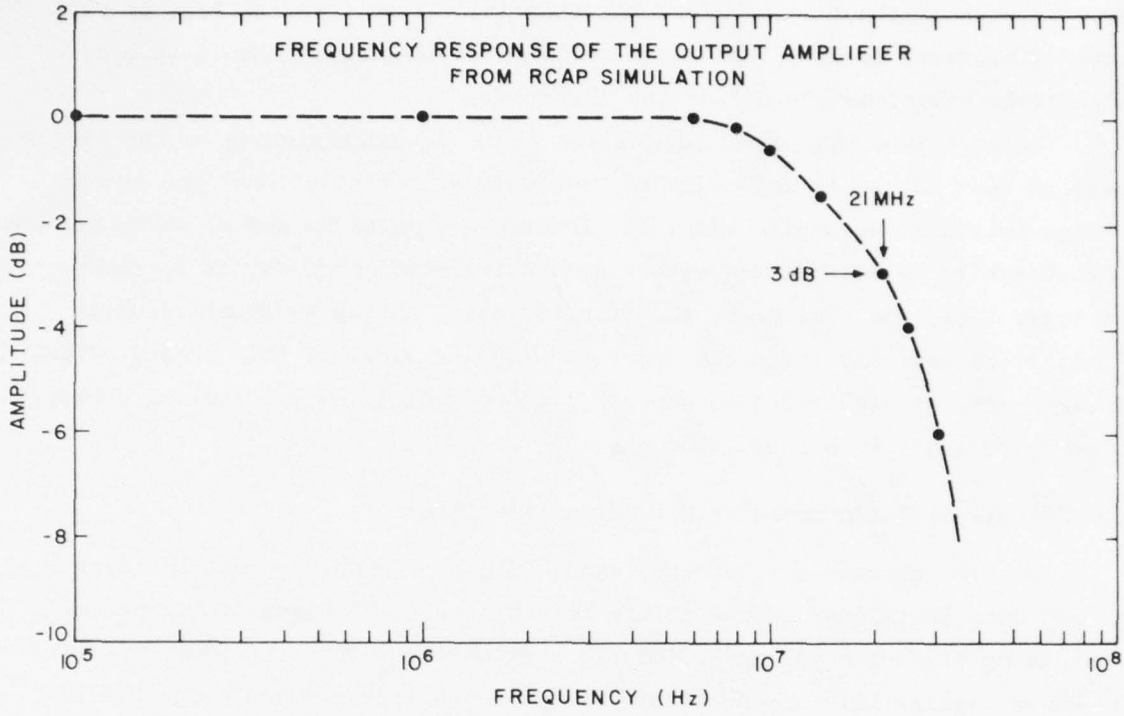


Figure 18. RCAP simulated frequency response of the output amplifier.

TABLE 2. TRANSISTOR DIMENSIONS USED IN RCAP SIMULATION

Transistor	W (mil)	L (mil)
Q_1	.4	.4
Q_2	1.4	.4
Q_3	1.2	.4
Q_4	5.0	.4
Q_5	20.0	.4
Q_6	.4	.4

Our experience with the photocomposition of the masks from three reticles shows that the alignment of these three reticles can be maintained to less than 0.02 mil. The most critical alignment from the processing point of view is on the first level of polysilicon. The photomicrographs illustrating the photocomposition alignment of a good mask for the first polysilicon level is shown in Fig. 19. The photomicrograph in Fig. 20 shows a similar situation for the second polysilicon mask. With more experience in mask photocomposition, we expect to be able to duplicate the almost perfect alignment (i.e., within $\pm$ 0.01 mil) as shown in Figs. 19(a) and 20(a).

Although photocomposition has been demonstrated, a new electron-beam exposure system will be available at RCA during the first quarter of 1978. It could be used to produce the masks for the 2200x96-element page reader and also will be considered for direct exposure of the photoresist on wafers.

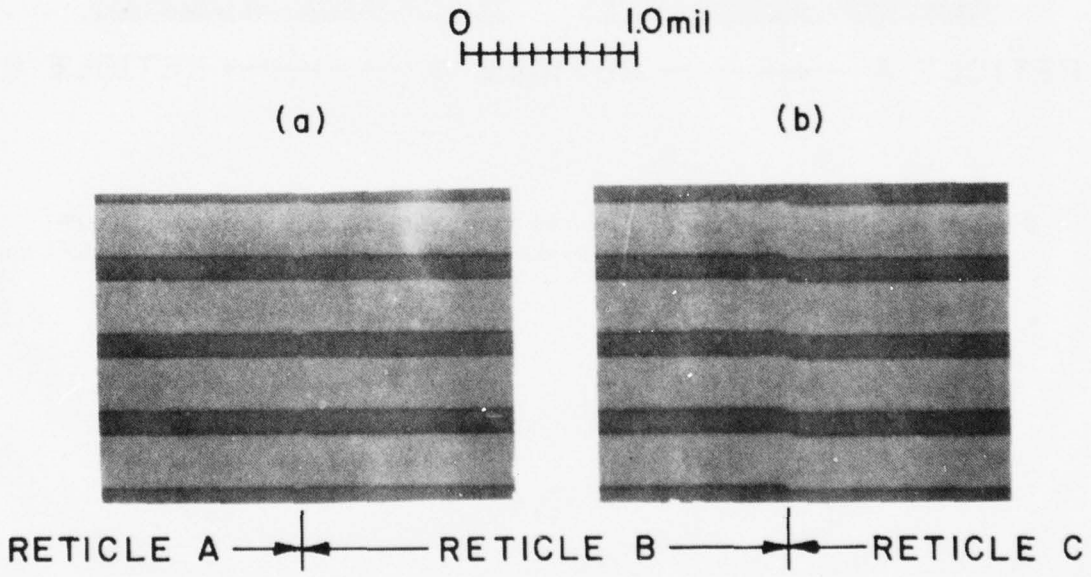


Figure 19. Photomicrographs of the two critical areas in photocomposition of the mask for the first level of polysilicon.

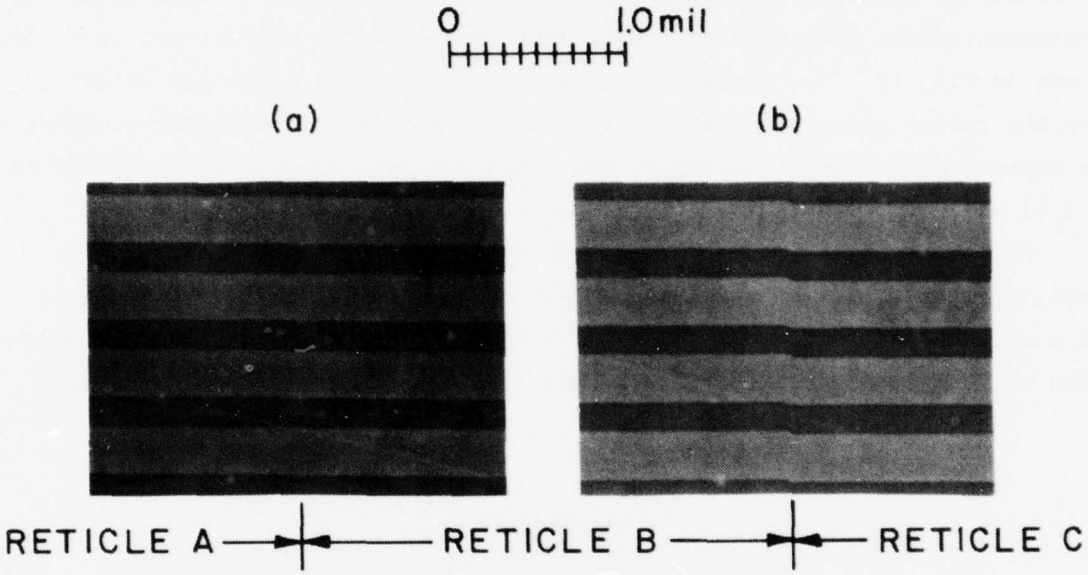


Figure 20. Photomicrographs of the two critical areas in the photocomposition of the masks for the second level of polysilicon.

SECTION IV

WAVEFORM GENERATOR

A. GENERAL DESCRIPTION

The TC1212 CCD page reader operates in a time delay and integration mode. Optical inputs incident on the TDI sensor section are integrated and subsequently transferred vertically to be stored in the first stage of the multiplexer. The vertical transfer of charge is accomplished with an electrode-per-bit clocking scheme. In the main array the signal charge undergoes a 4:1 multiplexing operation before it enters the temporary storage registers. From this temporary storage the charge packets are shifted into the output registers which, in turn, moves the charge horizontally to the output amplifier. The output amplifier and the floating diffusions of the output registers convert the charge to voltage, amplify it and perform a sample-and-hold function. The output shift registers for the 4:1 multiplexed page reader can be clocked at a maximum rate of 21 MHz. The output registers are 187 stages long and there are four output registers which give a total of 748 signal elements to be read out each TDI cycle.

All the timing of the sections described above are highly interdependent and extreme care must be used to ensure that the separate sections of the test chip will function together as a single unit. For this reason, a special-purpose waveform generator has been developed which can exercise the CCD page-reader test device with 4:1 multiplexing. Five different sets of waveforms must be generated.

- TDI electrode-per-bit
- 4:1 Multiplexer clocks
- Temporary storage clocks
- Transfer (into the output registers) clocks
- Output register clocks.

Each set of clocks is generated separately but synchronized with each other so that the transfer of the signal charge from one section to the next is uninterrupted.

These clock waveforms and the dc biases required to operate the TC1212 4:1 multiplexed CCD page reader are provided in two separate fixtures. The main part of the waveform generator is a logic/driver fixture shown in Fig. 21 which contains the logic circuit board and the clock driver board as well as the holder for the page-reader test chip. The printed circuit board connections for both boards are listed in Table 3. The logic circuit board supplies all the clock waveforms required for operation of the 4:1 multiplexed page reader. Standard TTL logic is employed in the derivation of the clock waveforms and the TTL logic levels are, in turn, translated to variable amplitude clock waveforms using MH0026 clock driver ICs located on the driver board. The location of the device holder (see Fig. 21) on the clock driver board was chosen, taking into account the necessity of short connecting leads from the clock drivers' output to the pin out of the device holder.

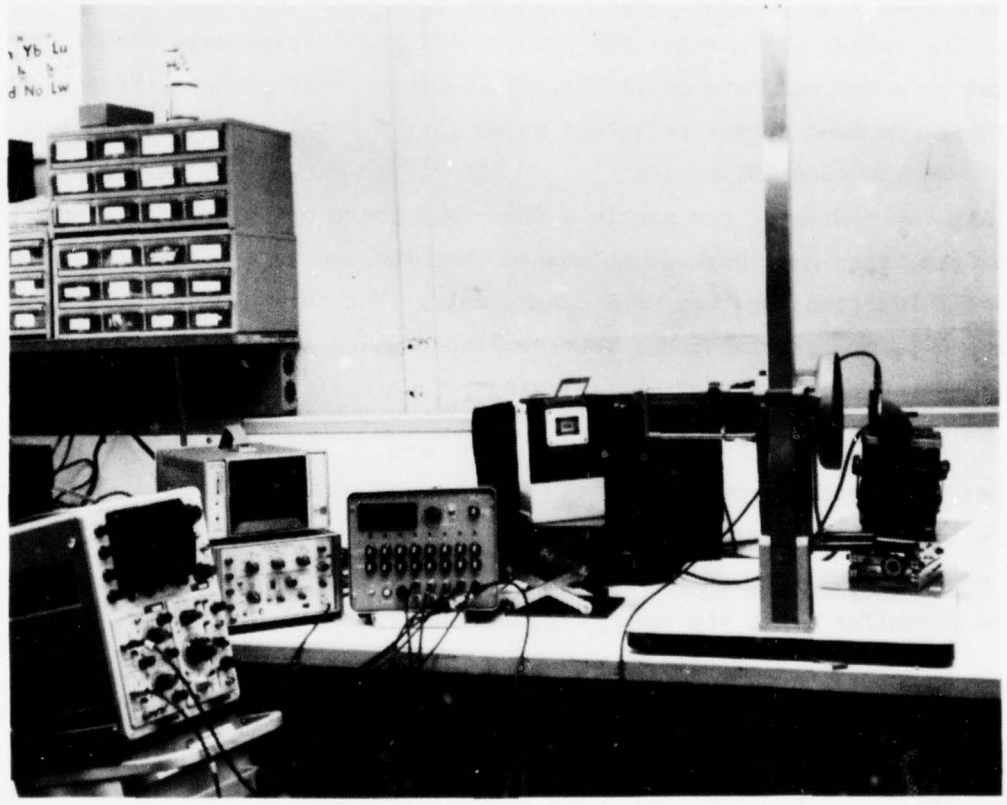


Figure 21. Optical test setup used for the scanning spot and the strobe optical tests.

TABLE 3. TC1212 - PIN ASSIGNMENTS AND CONNECTIONS LISTING

Function	PCB #1 Logic Card Pin #	PCB #2 Driver Card Pin #	Cable Conn.	Function	PCB #1 Logic Card Pin #	PCB #2 Driver Card Pin #	Cable Conn.
$\overline{401}$	A	E	---	M7	20	---	---
$\overline{402}$	B	V	---	V_{CC}	21	---	23
$\overline{403}$	C	19	---	V_S	---	S	10
$\overline{404}$	D	18	---	V_S'	---	W	12
$\overline{\theta}$	E	---	---	-10V	---	A	1
θ	F	X	---	V_{TFR}	---	B	2
V_{FC}	M	---	25	$V_{BIAS\ III}$	---	C	3
$\overline{402T}$	R	---	---	V_{CLK}	---	12	17
$\overline{S4}$,$\overline{S3}$	S	T	---	V_{STR}	---	2	13
$\overline{S2}$, $\overline{S1}$	T	D	---	$V_{BIAS\ I}$	---	3	14
402T	U	---	---	V_{DD1}	---	U	11
403T	V	---	---	$V_{BIAS\ II}$	---	17	22
$\overline{M6}$	W	4	---	V_{REF}	---	16	21
$\overline{M5}$	X	8	---	V_{DD}	---	10	15
$\overline{M2}$	Y	9	---	V_{RS}	---	M	6
GND ( )	Z	Z & 21	28	V_{SH}	---	L	5
SYNC IN	1	---	26	V_{DS1}	---	11	16
$\overline{\phi_{8-1}}$	2	6	---	$V_{\phi RS}$	---	22	24
$\overline{\phi_{6-7}}$	3	5	---	V_{P+}	---	N	7
$\overline{\phi_{4-5}}$	4	20	---	V_{FS}	---	H	4
$\overline{\phi_{2-3}}$	5	K	---	OUT 1	---	15	20
$\overline{T04}$	6	Y	---	OUT 2	---	14	19
T04	7	---	---	OUT 3	---	R	9
ϕ_{6-7}' (SYNC OUT)	11	---	27	OUT 4	---	P	8
$\overline{M3}$,$\overline{M4}$	12	J	---	REF	---	13	18
$\overline{404'}$	17	F	---				
$\overline{402'}$	18	7	---				
$\overline{M7}$	19	1	---				

The second part of the waveform generator is the power supply unit depicted in Fig. 21 which provides all dc voltage potentials and biases required for operating the device. The front panel controls can be used to adjust the clock waveform's amplitude and dc bias, the TDI and readout clock frequency and all dc voltages.

These two test fixtures were designed to be self-sufficient and operate the four 748x96-element 4:1 page-reader test structure without need of external power supplies. The following section will describe the design of the logic board and the CCD driver board which are contained in the main test fixture.

B. CIRCUIT DESCRIPTION

The TDI electrode-per-bit clock waveforms (ϕ_1 to ϕ_8) are derived from the SYNC IN pulses, which are externally applied to the logic board via the power supply fixture through the cable connector. Four of these incoming SYNC IN pulses constitute one TDI period ($\sim$30 μs). These TDI clock waveforms are generated by a four-bit shift register, NOR gate, one-shot multivibrator, and four NAND gates, (see Fig. 22). The SYNC IN pulses are used to clock the shift register and the NOR gate is used to ensure that only one bit or pulse cycles through the register. The bit starts at Q_o (high) then goes to Q_1, etc., until it reaches Q_3. Each time the bit reaches the fourth bit location (Q_3) of the shift register, the sequence begins again. The following describes the TDI waveform generation in more detail.

Assume an initial state of SR1 having all four outputs "low" or "zero." Under these conditions the three inputs of gate 031; Q_0, Q_1 and Q_2 represent zeros, thus due to the NOR function, the output of gate 031 yields a "one." This "one" enters the SR1 register by being applied simultaneously to the SR1 serial inputs, (J and $\bar{K}$, pins 2 and 3, respectively). Upon occurrence of a clock pulse, the "one" at the serial inputs gets shifted appearing at the Q_0 output. The inputs to gate 031 are now, high (Q_0), low (Q_1), low (Q_2). The 031 output now yields a zero. This value is supplied to the serial inputs of SR1. The occurrence of a clock pulse will shift the contents of the register one stage, thus Q_0 now yields a zero and output Q_1 represents a one. Q_2 as

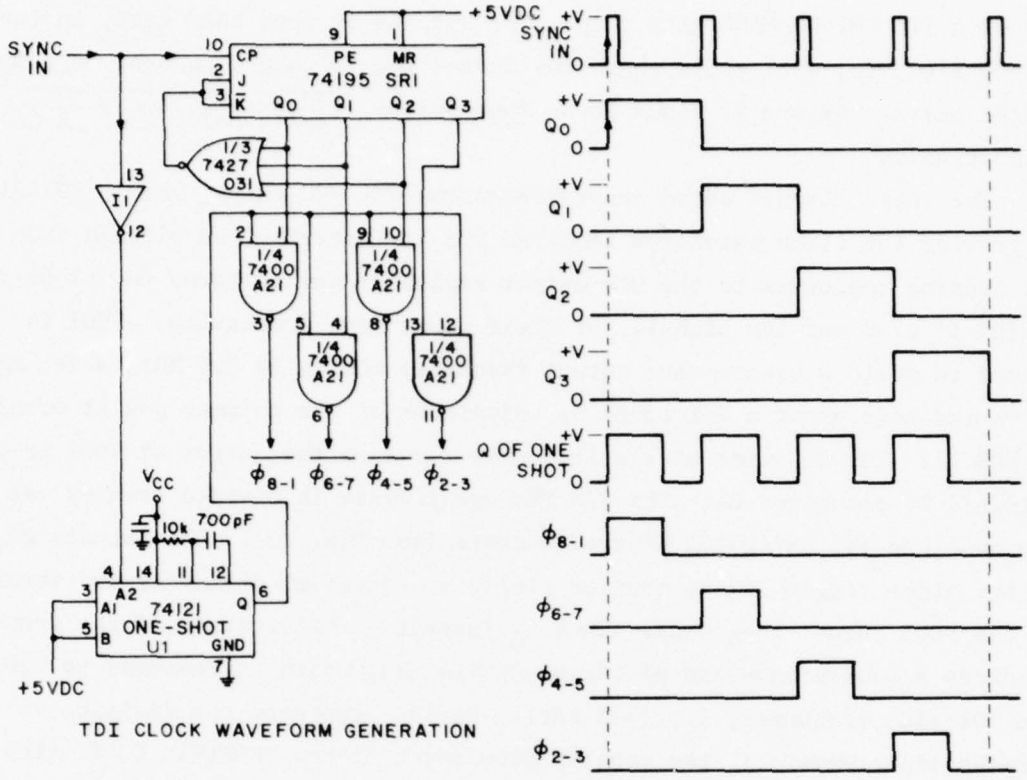


Figure 22. Circuit schematic and timing diagram of the TDI clock generation.

well as Q_3 are zero. In this fashion, every time a clock pulse appears the register will be loaded with the result of the NOR operation on the Q_0, Q_1 and Q_2 outputs of the shift register. Eventually, in the sequence, output Q_3 will yield a "zero." When this condition arises, a "one" loads the J and $\overline{K}$ inputs of SR1 and the sequence repeats itself with the occurrence of a clock pulse. The complemented form of the SYNC IN pulses trigger a one-shot TTL SN74121 multivibrator, U1, (see Fig. 22). The one-shot is biased such that each high to low transition of the clock, (complemented SYNC IN) sets the Q output (pin 6) high. The one shot remains in this stage for a period determined by external timing components, namely a 10 kΩ resistor, and a 700 pF capacitor. The period during which the Q output of the one-shot U1 is high must be less than the period between pulses of the clock. These transitions at the Q output of U1 are gated by a NAND function with Q outputs of SR1 by

use of a TTL SN7400 NAND gate chip. The outputs of each NAND gate, in the SN7400 TTL chip, will yield what constitutes the TDI clock pulses, in complemented pairs. Figure 22 shows these four pulses, $\overline{\phi_{8-1}}$, $\overline{\phi_{6-7}}$, $\overline{\phi_{4-5}}$, $\overline{\phi_{2-3}}$, respectively.

The logic circuit board incorporates two TTL VCO chips, module SN74S124, to provide the clock waveforms required for transferring the signals from the TDI sensing registers to the CCD output register; and in turn, the clock required to read out the signals for their subsequent processing. VCO1 is biased to yield a square-wave output frequency nominally 8.8 MHz, which may be varied over about a 2:1 range by adjustment of the trimmer pot R1 mounted on PCB #1. The midpoint of the frequency range at the output of VCO1 is determined by capacitor C1. The 8.8 MHz square-wave is divided down by use of two cascaded TTL SN74LS161 binary counters (see Fig. 23). The outputs of each of the eight stages of the counter yields a sequential divide-by-two version of the VCO1 output frequency. Thus Q_0 (output of first stage of the counter) produces a square-waveform of frequency 4.4 MHz, which corresponds to 128 times the TDI line frequency, f_L, ($\sim$35 kHz). Having completed the division of the 8.8-MHz input waveform, the counter provides a narrow TERMINAL COUNT (TC) pulse ($\sim$ 0.1 μs). The complemented version of this TC pulse is used to set the Q output of FF1 (1/2 SN7474 TTL) low. This transition at the Q output of FF1 (pin 5) is used to reset the eight-stage counter. At the same time, the transition at the $\overline{Q}$ output of FF1 (pin 6 is used to inhibit the operation of VCO1. Upon occurrence of the complemented version of pulse $\overline{\phi_{2-3}}$, this pulse clocks FF1 (pin 3), thus forcing its Q output, as well as the $\overline{Q}$ output, to change states. This action enables both, VCO1 and the eight-stage counter marking the start of another TDI clock cycle. Note, $\overline{\phi_{2-3}}$ marks the beginning of a TDI cycle. Figure 23 shows the logic diagram corresponding to the operation of VCO1, and the eight-stage counter.

Having obtained multiples of the TDI line frequency, f_L, the derivation of the waveforms necessary for the transfer and storage of signal charge from the TDI array to the CCD output register is accomplished by means of TTL logic modules. Figure 23 shows the logic circuit diagram which generated the waveforms

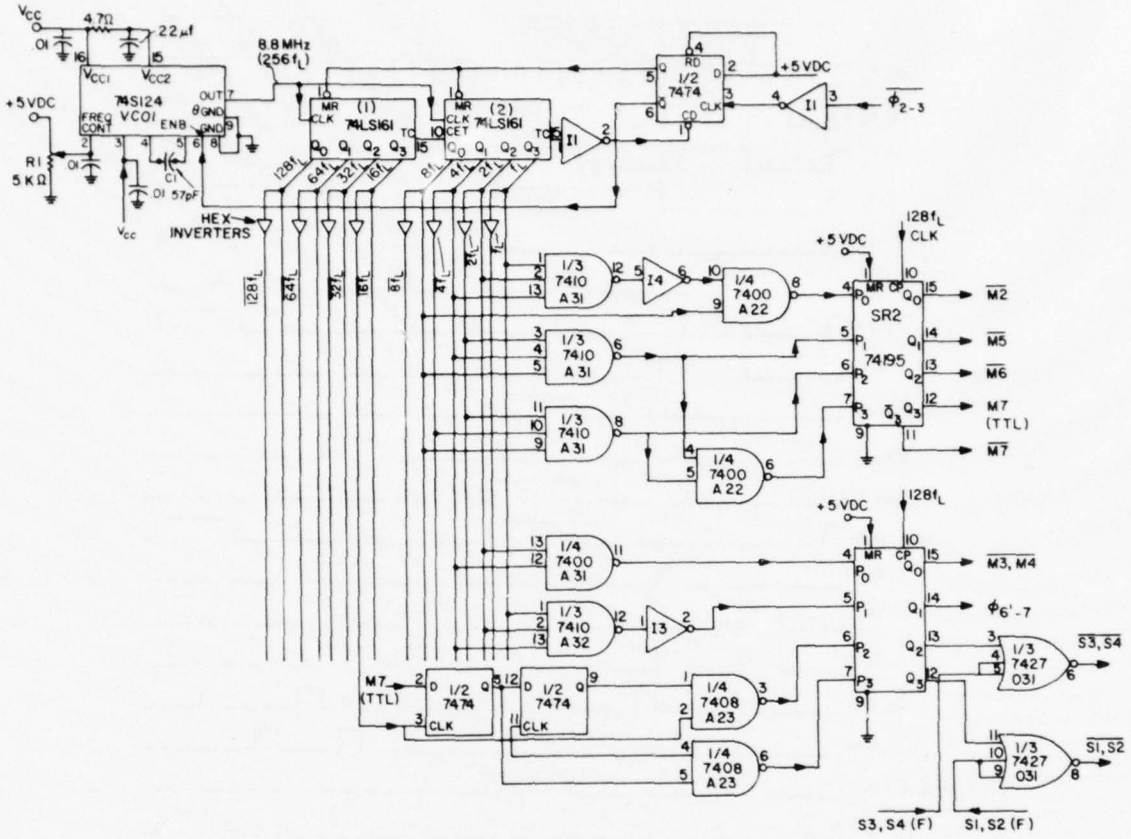


Figure 23. Circuit schematic for the multiplexer and temporary storage register clock generation.

required as shown in the timing diagram, Fig. 24. The multiplexer gates, M1 through M7, are pulsed sequentially in order to perform the multiplexing scheme required during operation of the device. Also shown in these figures is the generation of pulses S1, S2, S3, and S4 used for temporary storage prior to readout. Registers SR2 and SR3 (SN74195 modules) are used for the purpose of overriding possible unwanted transitions that may occur while deriving the various waveforms. After the multiplexer clock waveforms and the temporary storage register waveforms have been generated, the transfer and readout clock waveforms must be generated as described in the next paragraphs.

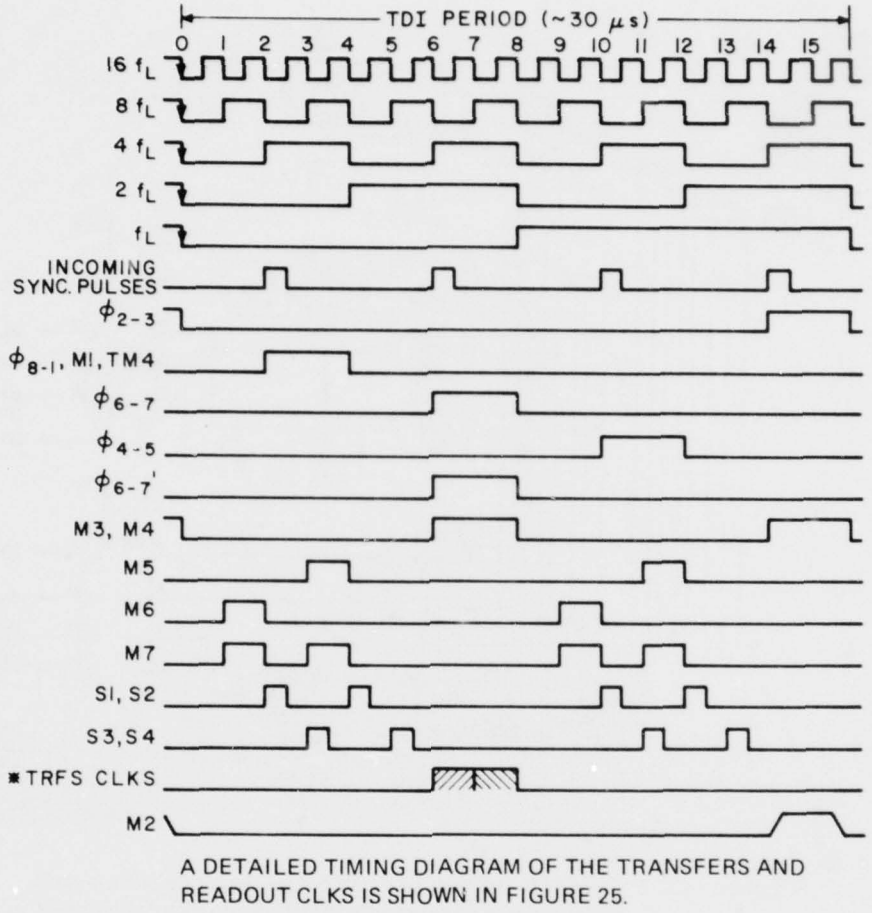


Figure 24. Timing diagram for the multiplexer and temporary storage register clocks.

The occurrence of ϕ_{6-7}' initiates the transfer and readout period. Figure 25 represents the timing diagram required for this task. The derivation of these waveforms is depicted in Fig. 26. Electrodes S1, S2, S3, and S4 as well as T04, 402' and 404', are pulsed sequentially in order to load the signals onto the CCD output register. Having accomplished this transfer the output register is clocked by pulses 401, 402, 403, and 404, thus transferring the signals horizontally for their subsequent sensing and amplification.

The signals are read out at a much faster rate than the TDI frequency. VCO2, (TTL SN74S124), controls the readout frequency. VCO2 is biased to

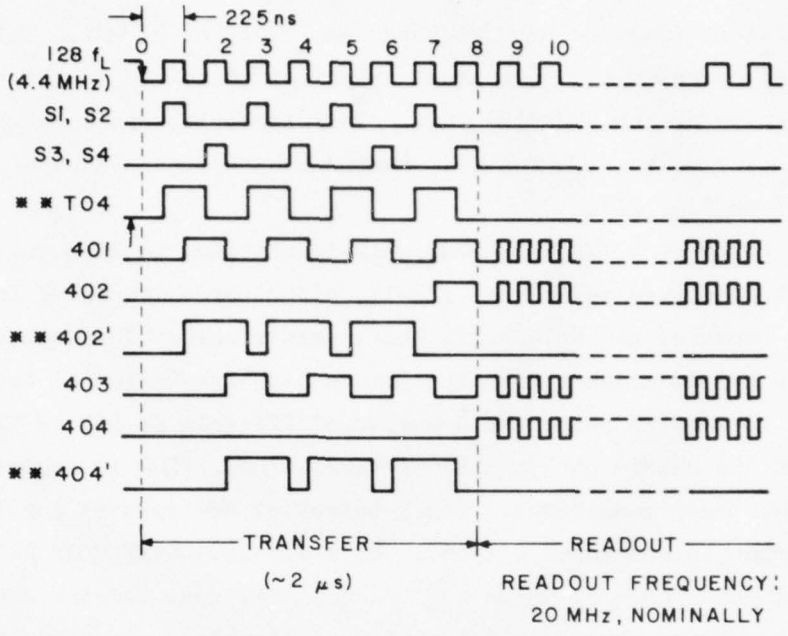


Figure 25. Timing diagram for the transfer and readout clocks of the output register.

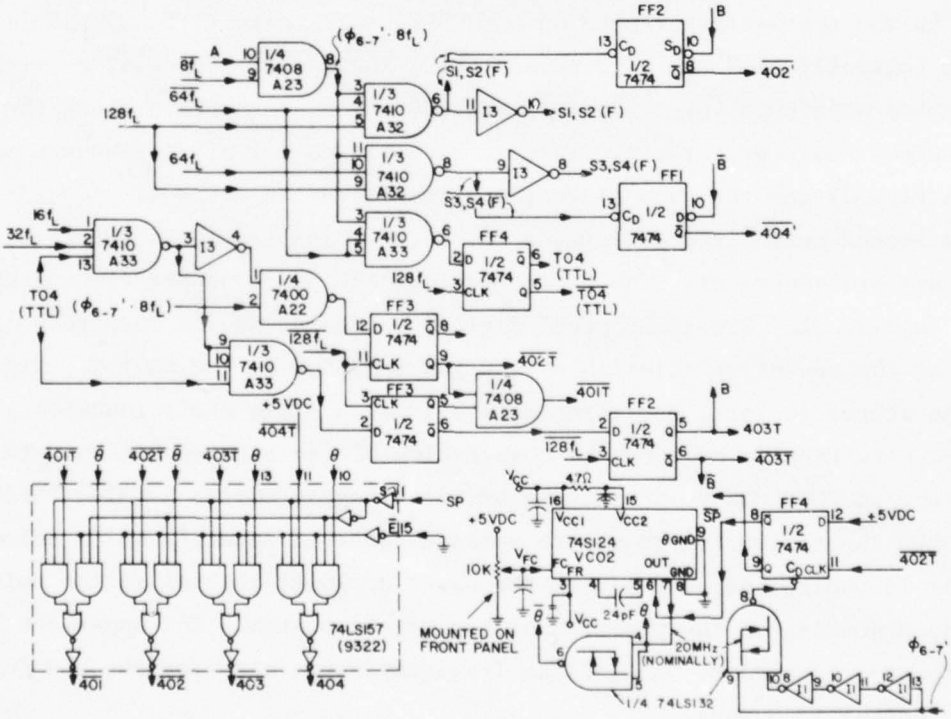


Figure 26. Circuit schematic for the output register clock generation.

produce a square-wave output frequency nominally at 21 MHz. This frequency is established by means of an external capacitor connected to the external timing component pins of the SN74S124 VCO2. This frequency can be varied over a 3:1 range by means of the V_{FC} control mounted in the front panel of the power supply fixture, (see Fig. 21).

One fourth of a TTL SN74LS132 chip is utilized to NAND together with the ϕ_{6-7}' with a delayed version of itself, after three stages of inversions performed by means of the SN7404 TTL Hex Inverter chip. This operation yields a spike ($\sim$50 μs) coincident with the low to high transition of the ϕ_{6-7}' pulse. The spike is used to reset the $\overline{Q}$ output of FF4 (pin 8; 1/2 SN7474) high which is tied to the enable pin (pin 6) of VCO2. Thus, VCO2 is inhibited from operation, under these conditions. The Q output of FF4 (pin 6) labeled SP is tied to the common select input 8 (pin 1) of a TTL SN74LS157 QUAD 2-INPUT MULTIPLEXER chip. The occurrence of pulse $\overline{402T}$ clocks FF4, thus forcing the $\overline{Q}$ output low and Q high. Under these conditions VCO2 is enabled, producing a nominally 21-MHz square-wave output. This output waveform, as well as its complemented version, are obtained from a 1/4 SN74LS132 chip used as an inverter; and they are the $\overline{\theta}$ and θ waveforms, respectively. These two waveforms, in turn, are applied to the appropriate inputs of the MULTIPLEXER chip (TTL SN74LS157) where they are logically combined with pulses $\overline{401T}$, $\overline{402T}$, $\overline{403T}$, and $\overline{404T}$ to yield the complemented waveforms $\overline{401}$, $\overline{402}$, $\overline{403}$, and $\overline{404}$ which are used to clock the TC1212 output register. The clock driver schematics for all the waveforms are shown in Fig. 27 and the chip connections are listed in Table 4.

The second test fixture provides all of the bias levels to the logic/driver waveform generator. The front panel of the power supply fixture can be seen in Fig. 21. The front panel digital voltmeter may be used to monitor any one of the seventeen adjustable voltages supplied by the tester. Figure 28 shows the schematic for these circuits and Table 5 lists their functions. Voltmeter selection is made by the combination of the eight-position rotary switch labeled "DVM CONTROLS" and the adjacent toggle switch labeled "UPR" and "LWR". LED lights located above the voltage controls identify which column the voltmeter is monitoring, and either the upper or lower control in the column is measured, depending on the position of the toggle switch. The upper 8th column control is used to monitor the frequency range bias for the VCO supplying the readout frequency.

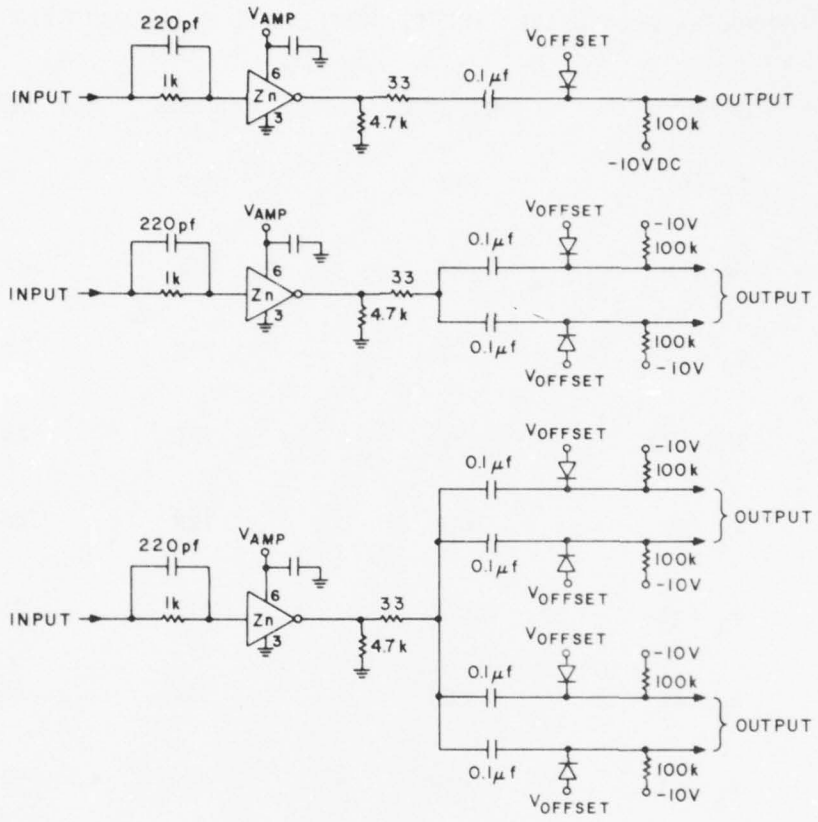


Figure 27. Clock driver circuit schematic for the TC1212 waveforms. See Table 4 for the appropriate input, output, etc., and chip numbers.

The output signals from the CCD page reader are taken from the five BNC receptacles in the lower selection of the front panel, and are labeled OUT1, OUT2, OUT3, OUT4, and REF. There are also two separate BNC connectors labeled V_S and V_S', which can be used if an electrical signal is to be applied to the output register. The V_S is connected to the source diffusion of the first four channels and V_S' is connected to the reference register -- all are ac-coupled and V_{REF} is the bias voltage. The BNC connector labeled "SYNC IN PULSES" accepts the synchronizing pulses necessary for the generation of the TDI clocks as discussed above. This SYNC IN signal should be compatible with TTL logic levels. Adjacent to the SYNC IN connector is the SYNC OUT point. The SYNC OUT provides a TTL compatible, positive going pulse whose duration is sufficient to provide a trigger source which occurs once every TDI cycle.

TABLE 4. MMH0026 CLOCK DRIVER INPUT, OUTPUT, AND BIAS CONNECTIONS*

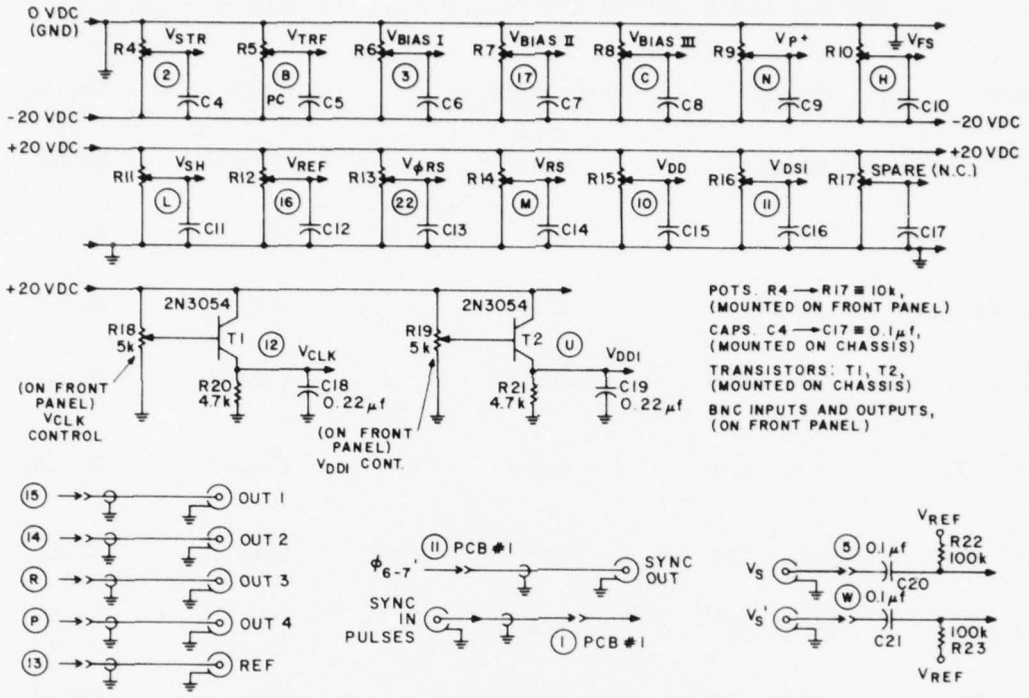
INPUT	OUTPUT	AMPLITUDE	OFFSET	DRIVER
$\overline{\phi_{8-1}}$ (2)	ϕ_1 (7)	CLK	STR	Z9(c)
$\overline{\phi_{8-1}}$ (2)	M1 (7)	CLK	STR	Z9(c)
$\overline{\phi_{8-1}}$ (2)	ϕ_8 (7)	CLK	TRF	Z9(c)
$\overline{\phi_{8-1}}$ (2)	TM4 (7)	CLK	TRF	Z9(c)
$\overline{\phi_{2-3}}$ (4)	ϕ_2 (5)	CLK	TRF	Z5(b)
$\overline{\phi_{2-3}}$ (4)	ϕ_3 (5)	CLK	STR	Z5(b)
$\overline{\phi_{4-5}}$ (2)	ϕ_4 (7)	CLK	TRF	Z4(b)
$\overline{\phi_{4-5}}$ (2)	ϕ_5 (7)	CLK	STR	Z4(b)
$\overline{\phi_{6-7}}$ (4)	ϕ_6 (5)	CLK	TRF	Z8(b)
$\overline{\phi_{6-7}}$ (4)	ϕ_7 (5)	CLK	STR	Z8(b)
$\overline{M2}$ (2)	M2 (7)	CLK	BIAS II	Z5(a)
$\overline{M3}$, $\overline{M4}$ (4)	M3 (5)	CLK	TRF	Z6(b)
$\overline{M3}$, $\overline{M4}$ (4)	M4 (5)	CLK	STR	Z6(b)
$\overline{M5}$ (2)	M5 (7)	CLK	TRF	Z6(b)
$\overline{M6}$ (4)	M6 (5)	CLK	TRF	Z7(b)
$\overline{M7}$ (2)	M7 (7)	CLK	STR	Z7(b)
$\overline{S1}$, $\overline{S2}$ (2)	S1 (7)	CLK	TRF	Z8(b)

TABLE 4. MMH0026 CLOCK DRIVER OUTPUT AND BIAS CONNECTIONS* (Continued)

INPUT	OUTPUT	AMPLITUDE	OFFSET	DRIVER
$\overline{S1}$, $\overline{S2}$ (2)	S2 (7)	CLK	STR	Z8(b)
$\overline{S3}$, $\overline{S4}$ (4)	S3 (5)	CLK	TRF	Z1(b)
$\overline{S3}$, $\overline{S4}$ (4)	S4 (5)	CLK	STR	Z1(b)
$\overline{T04}$ (2)	T04 (7)	DD1	BIAS I	Z3(a)
$\overline{402^{1}}$ (2)	$402'$ (7)	DD1	BIAS I	Z10(b)
$\overline{404^{1}}$ (4)	$404'$ (5)	DD1	BIAS I	Z10(b)
$\overline{401}$ (4)	401 (5)	CLK	TRF	Z9(b)
$\overline{401}$ (4)	$401'$ (5)	CLK	TRF	Z9(b)
$\overline{402}$ (2)	402 (7)	CLK	STR	Z2(b)
$\overline{403}$ (4)	403 (5)	CLK	TRF	Z2(b)
$\overline{403}$ (4)	ϕ_{OUT}(5)	CLK	TRF	Z2(b)
$\overline{403}$ (4)	G2 (5)	CLK	BIAS III	Z2(b)
$\overline{404}$ (2)	404 (7)	CLK	STR	Z1(a)
$\bar{\phi}$ $\overline{(4)}$	ϕ_{RS} (5)	CLK	$V_{\phi RS}$	Z4(a)

*Refer to Figs. 26(a), (b), or (c) for the circuit schematic.

The driver designation refers to the appropriate figure. The numbers in parentheses in the INPUT and OUTPUT columns refer to pin numbers on the MM0026 clock driver chips. The numbers in the DRIVER column refer to the chip numbers, i.e., Z9 refers to the driver chip designated number 9; the letter refers to the circuit schematic in Fig. 27.



NOTE: CIRCLED ENTRIES REFER TO PIN LOCATION IN PCB # 2, UNLESS SPECIFIED DIFFERENTLY.

Figure 28. Circuit schematic for the power supply.

This section has described the waveform generator which provides the five sets of clocks needed to drive the TC1212 748x96-element page reader with 4:1 multiplexing. This waveform generator has been used to operate the output registers with electrical input, the entire device using both a scanning light spot and a strobed optical input. These tests will be discussed in the next section.

TABLE 5. BIAS ADJUSTMENTS

Control		Function	Range (DC Volts)
R4.	V_{STR}	Storage-Gate Bias (ϕ_1, ϕ_3, ϕ_5, ϕ_7, M1, M4, M7, S2, S4, 402, 404)	-20 to 0
R5.	V_{TFR}	Transfer-Gate Bias (ϕ_2, ϕ_4, ϕ_6, ϕ_8, M3, M5, M6, S1, S3, 401, 403, TM4, ϕ_{out}, 401')	-20 to 0
R6.	$V_{BIAS\ I}$	Transfer to output reg. Gate Bias (402', 404') / Storage Gate Bias (T04)	-20 to 0
R7.	$V_{BIAS\ II}$	MUX Transfer Gate (M2)	-20 to 0
R8.	$V_{BIAS\ III}$	Input Gate Bias (G2)	-20 to 0
R9.	V_{P+}	Substrate Bias	-20 to 0
R10.	V_{FS}	*Field Shield Bias*	-20 to 0
R11.	V_{SH}	Sample & Hold Gate Bias (S/H)	0 to +20
R12.	V_{REF}	CCD Source Bias	0 to +20
R13.	$V_{\phi RS}$	Reset Gate Bias	0 to +20
R14.	V_{RS}	CCD Drain Bias	0 to +20
R15.	V_{DD}	Signal Input Bias (V_{D1}, V_{D2}, G1)	0 to +20
R19.	V_{DS1}	Aux. Clock Amplitude (402', 404', T04)	0 to +20
R18.	V_{CLK}	Main Clock Amplitude (M1, M3 to M7, ϕ_1 to ϕ_8, TM4, 401 to 404, 401', 402', 404', S1 to S4, ϕ_{RS}, ϕ_{out}, G2)	0 to +20
R2.	V_{FC}	TDI Freq. Control (front panel)	0 to +5
R7.	(SPARE)		
BNC RECEPTACLES		INPUT SIGNAL TO REGISTER (V_S, V_S') OUT1, OUT2, OUT3, OUT4, REF. SYNC OUT (ϕ'_{6-7}) SYNC IN (INCOMING SYNC. PULSES)	

SECTION V

EXPERIMENTAL RESULTS

A. PROCESSING OF PAGE-READER TEST ARRAYS

Three processing runs were made of the page-reader test arrays, TC1212, using the two-level polysilicon buried-channel CCD technology modified to improve yield for large area arrays. Each processing run had eight starting wafers and each wafer had twelve possible page-reader test chips. The wafer is shown in Fig. 29 where the twelve devices can be seen in the central portion of the wafer. Around the periphery of the wafer, the reticle which contains most of the test devices has been stepped in place of the normal reticle to fully utilize the wafer area.

The first two runs did not produce any useful 748x96-element test chips. However, enough information was obtained from these runs that the process could be optimized, and the third run produced 21 devices (from a total of 96 possible -- 20%) which passed static testing. Ten of these devices were damaged in scribing and bonding. Finally, 11 devices were obtained which were usable. All eleven of these devices produced some optical output, which will be discussed later in this section. These devices were bonded in 56-pin flatpack packages, which require plastic holders. The flatpack and its holder are shown in Fig. 30. The bonding diagram is shown in Fig. 31.

B. ELECTRICAL AND OPTICAL TESTS

The testing of the 748x96-element TDI-CCD page-reader devices with 4:1 output multiplexing included the measurement of the channel potentials of the output registers as a function of the gate voltages, demonstration of the operation of the 4:1 charge multiplexer, initial optical testing of the operation of the array with a scanning light spot, and the demonstration of the operation of the page-reader test array by displaying on a TV monitor the optical images projected on the TDI array. This last test demonstrated the correct operation of all the parts of the 748x96-element TDI-CCD line sensor with 4:1 multiplexed output.

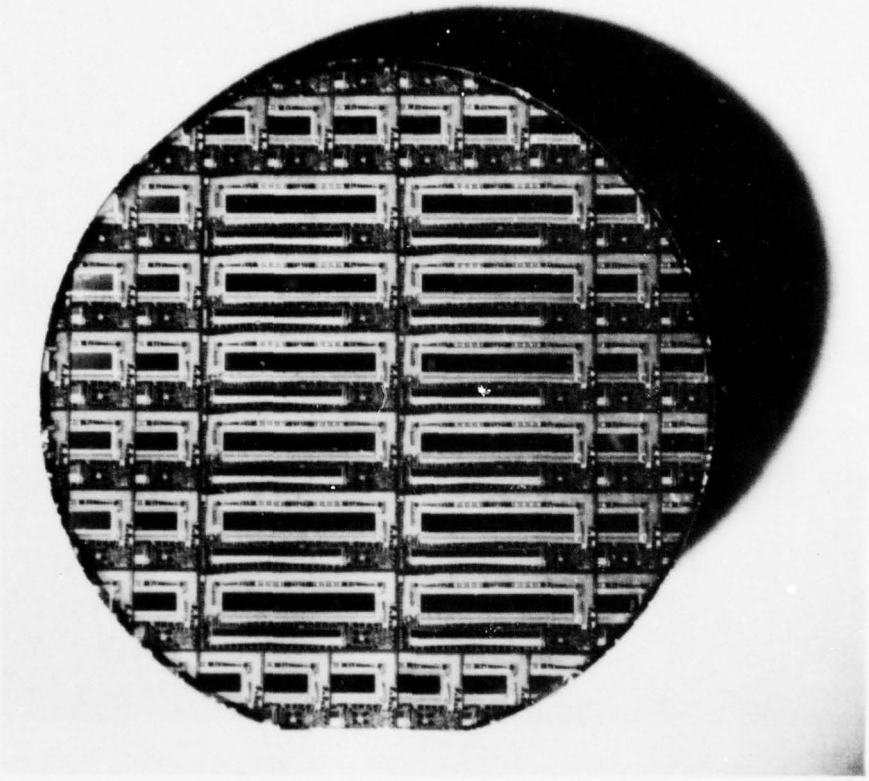


Figure 29. Photomicrograph of a wafer of the TC1212 748x96 TDI-CCD page-reader test chip showing the 12 full devices in the central portion of the wafer and the test structures in the periphery.

1. Channel Potential Plots

The proper operating voltages for the clock waveforms of a CCD can be obtained by determining the channel potential under the polysilicon gates as a function of the gate voltage referenced to the substrate. The CCD can be viewed as a long channel MOSFET with multiple gates and when operated in this mode a channel potential vs gate voltage plot can be determined. For the 748x96-element CCD page reader with 4:1 multiplexing the plot is even more useful since there are a total of 20 clock phases whose amplitude and offset

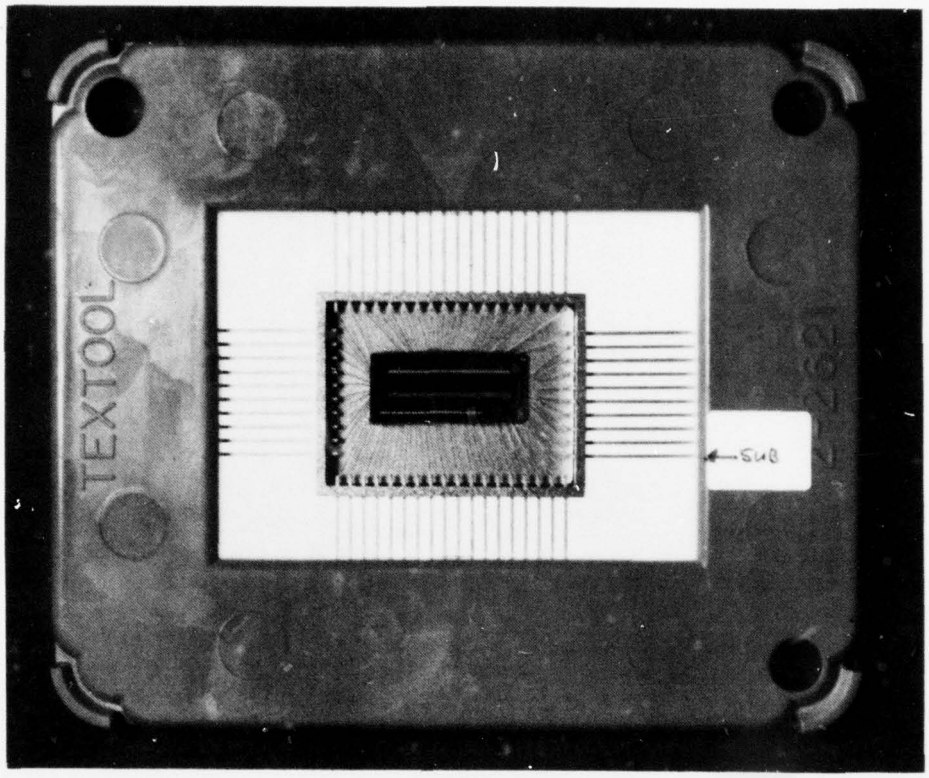


Figure 30. Photomicrograph of a packaged device in the plastic holder.

voltages must be determined. Specifically, the multiplexing concept proposed and used in this page reader test chip requires proper adjustment of the clock voltage levels which can be easily determined. The channel potential plot was determined from the output register section as follows:

(1) Apply +20 V to the reset drain (V_{RS}) of the output register.
(2) Apply +20 V to all gates except the one where potential plot is being determined.

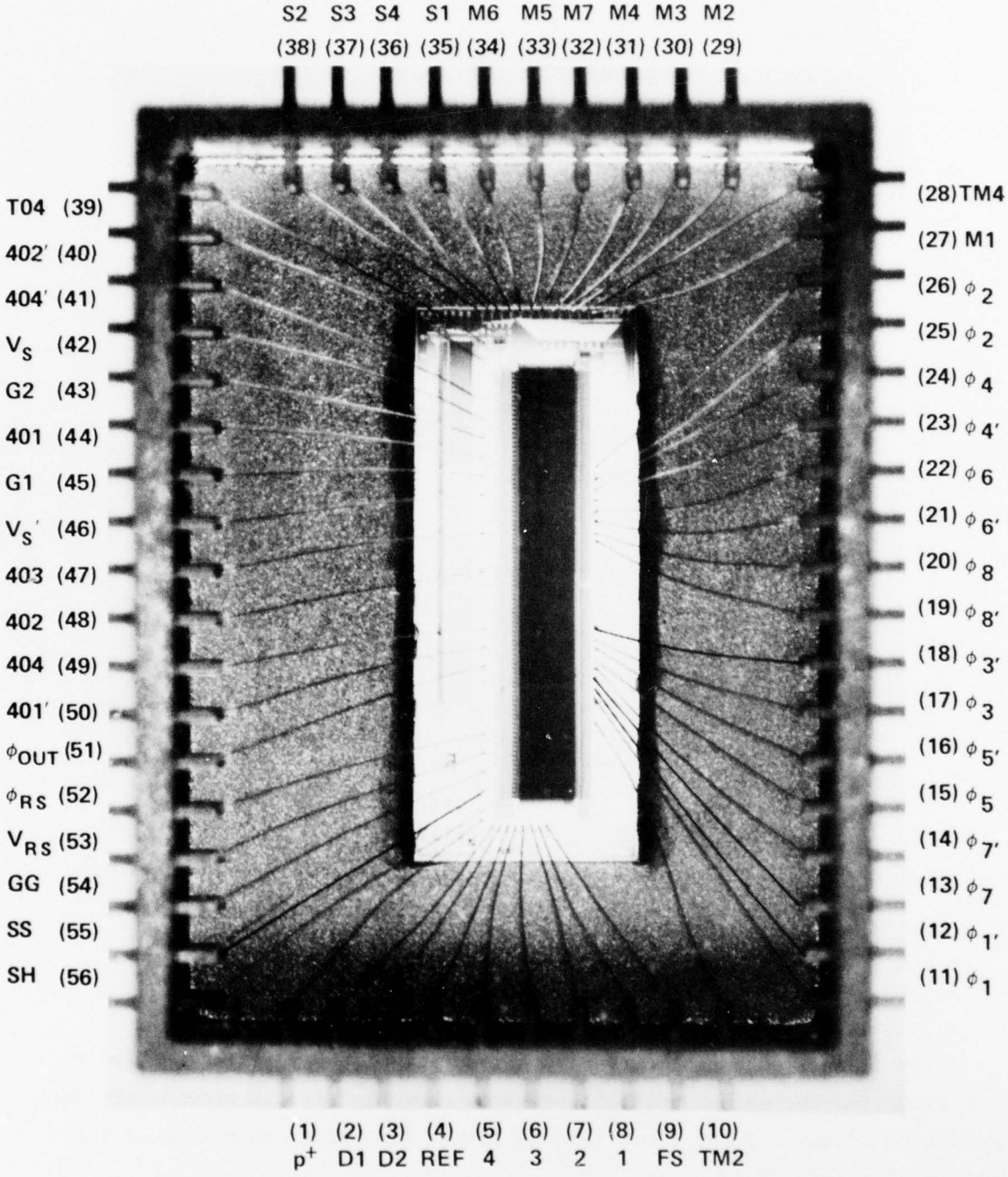


Figure 31. Bonding diagram for the TC1212 748-96-element TDI-CCD page-reader test chip.

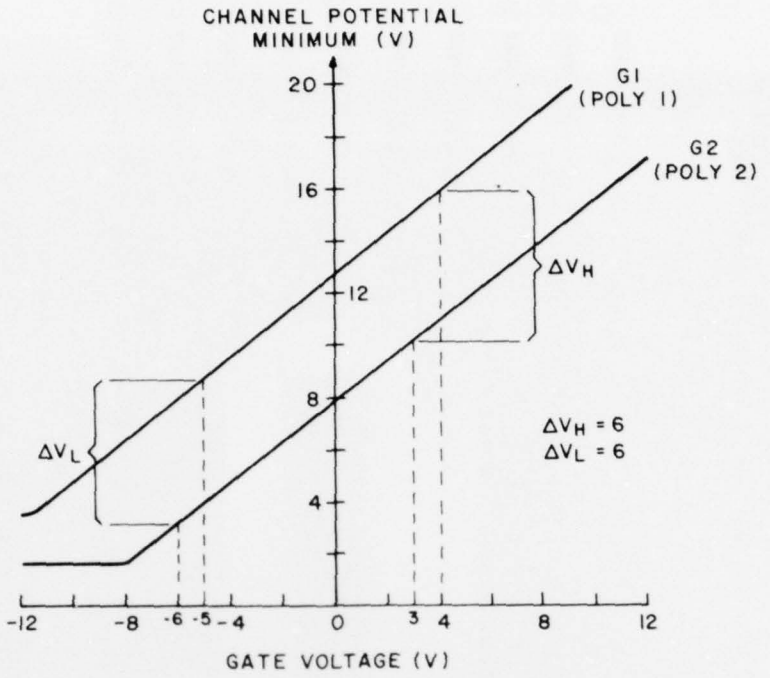


Figure 32. Channel potential vs gate voltage plot used to determine the optimum gate voltages. ΔV_H and ΔV_L are the well sizes (in volts) at the high and low clock levels.

(3) Apply a voltage V_G to this latter gate.

(4) Determine the source voltage (V_S) required to just turn off the transistor. This voltage is the channel potential of the CCD well under the gate when no charge exists in the well.

(5) Repeat steps (3) and (4) until a sufficient number of points have been determined.

The channel potential curves as a function of the voltages applied to the first and the second polysilicon gates shown in Fig. 32 provide the data needed to adjust all the clock voltage levels for proper operation of the page-reader test array.

2. 4:1 Multiplexer Test Circuit

The TC1212 CCD page-reader test chip contains several test structures which can be used to facilitate the testing and evaluation of the main 4:1 multiplexed page-reader array. Among these is the 4:1 and 2:1 multiplexer test circuit which can be used to investigate the novel multiplexing concepts being used in the page reader. This multiplexer test circuit allows the optimum voltages and waveforms to be determined for the multiplexing without having to be concerned with the other concepts being introduced in the main array. The 4:1 multiplexer is a duplicate of that used in the main array as shown in Fig. 33, and also has the four-stage temporary storage register.

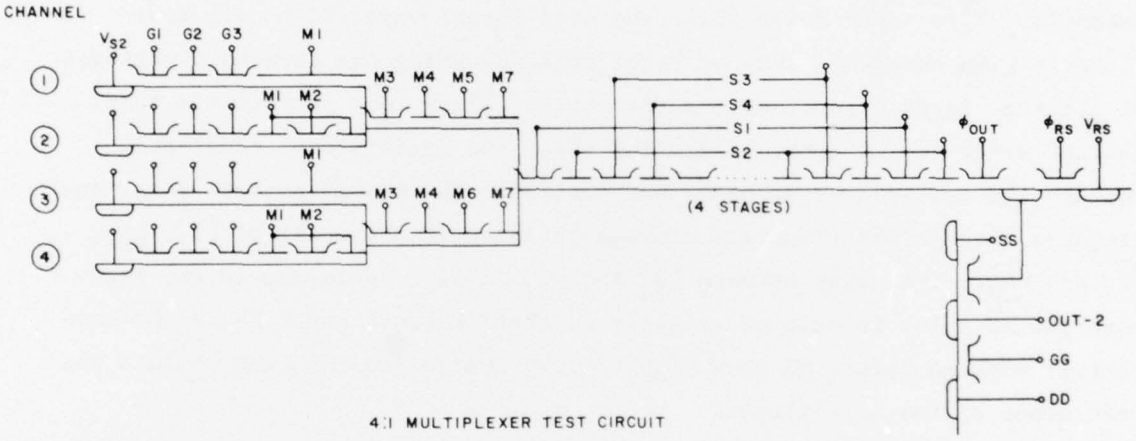


Figure 33. Schematic drawing at the 4:1 multiplexer test structure with the three gate input structure, the four-stage temporary storage section, and the output circuit.

The 4:1 multiplexer test circuit has a common source diffusion, V_{S2}, to all four channels. All four channels have three common gates at the input, G1, G2, and G3, which can be used to inject charge from the source. Following the input gate structure is the 4:1 multiplexer structure with the gates M1 through M7. After the final multiplexer gate (M7) is the four-stage temporary storage register. This register is a duplicate of the temporary storage

register in the full array, which stores the signal charge so that a rapid transfer can be made into the output register independent of the multiplexer operation. The multiplexer test circuit has been included to determine the voltages and timing required for the proper operation of the multiplexer and the temporary storage register in the 748x96 array. Following the temporary storage register is an output section which includes an output gate (ϕ_{OUT}), a reset gate (ϕ_{RS}), a floating diffusion and reset drain (V_{RS}). Finally, there is an amplifier with an on-chip load. The operation of the multiplexer requires 14 phase clocks. The waveforms used to evaluate this structure are shown in Fig. 34, and the voltage levels used in Table 6. The output obtained is shown in Figure 35.

The output shows four bits out for one input pulse to all four input channels. This input pulse fills the well formed under G2 in all four channels with charge packets of equal size (assuming the threshold voltages of all four input structures are the same). These four packets are then shifted under the M1 gate. Following this, the packets are transferred through the multiplexer as describer earlier. The charge packets enter and transfer through the temporary storage register in the order of (1), (3), (2) and (4). The delay between (3) and (2) in Fig. 34 is due to the fact that the M2 pulse is delayed slightly so that the well under M4 can be completely emptied before M2 goes high to dump charge from (2) and (4) into the last stage of the multiplexer.

It is seen that the four output pulses are not equal in Fig. 35. One reason for this is that the threshold voltages of the gates are not equal, but another is that the waveshapes of the multiplexer clocks may not be optimum, i.e., the fall time of the M2, M5, and M6 may not be slow enough to completely transfer the charge out of the multiplexer. The major limitation of this test, however, has been that the 4:1 charge multiplexer was tested on the wafer with the probe-card inputs. The test circuit must be bonded in an IC package before a complete test of this charge multiplexing circuit can be accomplished.

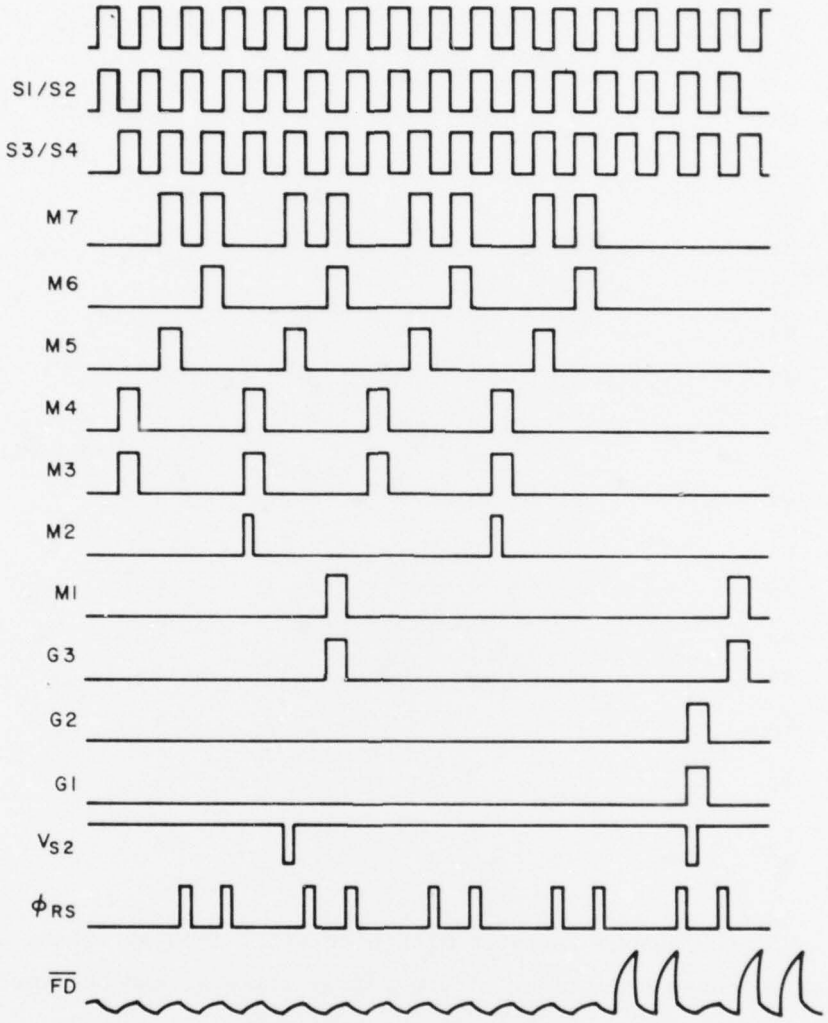


Figure 34. Timing diagram for the 4:1 multiplexer test chip.

3. 748x96 4:1 Multiplexed Page-Reader Test Array

The output register of the 748x96-element 4:1 multiplexed test array has been designed so that the four data channels have a common source and two common input gates. The reference channel has a separate source, but shares the two input gates with the four data channels. This facilitates the testing of

TABLE 6. CLOCK VOLTAGES USED FOR THE 4:1 MULTIPLEXED TEST CIRCUIT

	Amplitude	Offset
V_{S2}	15	+ 4
G1	9	- 8
G2	9	- 3
G3	9	- 7
M1	9	- 5
M2	9	- 9
M3	9	-12
M4	9	-10
M5	9	- 7
M6	9	-12
M7	9	- 2
S1	9	-10
S2	9	- 1
S3	9	- 8
S4	9	- 0
ϕ_{OUT}	-	- 4
ϕ_{RS}	9	-12
V_{RS}	-	+15

the operation of the output register with electrical inputs. Thus, the optimum clock voltages and timing of the output register can be determined independently of the other sections of the test chip.

From the testing of the output register the optimum voltages for the gates have been determined (401, 401', and 403 swing from -6 to +3 V and 402 and 404 swing from -5 to + 4 V). These voltages are shown on the channel potential plots and it is seen that the device does not operate in the bucket-brigade mode with these clock voltages. In fact, the barrier of the receiving phase is about one volt below the storage well in the transfer phase.

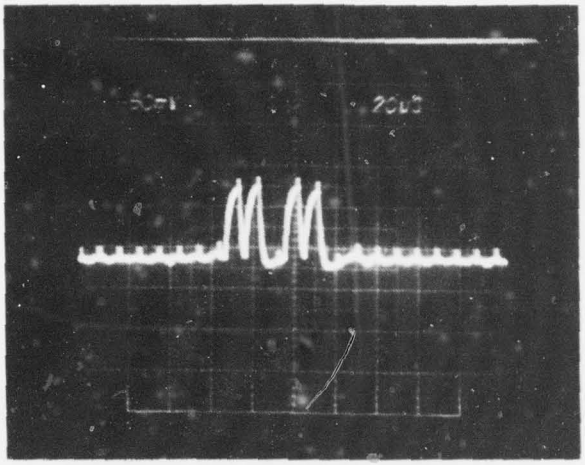


Figure 35. 4:1 multiplexer test chip showing one pulse into the test chip and the resulting four output pulses.

The charge transfer losses of the output registers were measured by injecting electrical inputs to all four registers in parallel. The results showed that the charge-transfer losses were on the order of 10^{-4} per transfer or less. Since each output register has only 187 stages it is difficult to measure charge-transfer losses. From our previous data, however, buried-channel CCDs fabricated with essentially the same process, we expect the charge-transfer loss to be about $2x10^{-5}$ per transfer for operation without fat zero, and about 10^{-5} per transfer for operation with fat zero.

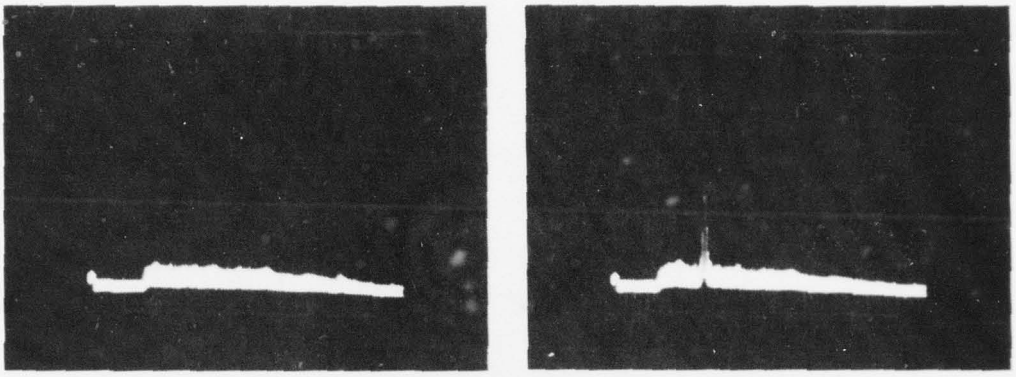
Initial optical test of the 748x96-element page-reader test array were done with a movable optical spot focused on the TDI imaging section. This light spot had a size of about 4 mil and could be manipulated in the x, y, and z direction. The purpose of this initial test was to demonstrate horizontal resolution capability of the imaging section of the test chip and to verify that the multiplexer functioned properly in the page reader.

The waveform generator described in Section IV was used in both of the optical tests which are described here. Figure 36 shows the results obtained

from these initial moving spot optical tests. Fig. 36(a) shows the signal from one of the output registers before the light spot had been positioned on the TDI imaging section. Fig. 36(b) shows the spot positioned near the right side of the array. The spot was then slowly moved across the TDI section until the left side of the chip was reached. Figures 36(c) and 36(d) show the spot in the center and near the left side of the chip, respectively. Since the spot is nearly circular and the test chip was operating in the TDI mode, the amplitude of the five output pulses are different. When the spot is centered on one channel, the output from this channel will have a maximum amplitude. The amplitude of the output from the channels on either side of this center channel will then be less than the maximum, and decrease to zero for channels at the edge of the spot. The lack of symmetry in the output pulses is due to the imperfect circular shape of the spot.

The proper operation of the 4:1 multiplexer section and the horizontal response capability of the TDI section was shown by the following test. As the spot was focused on the TDI section and centered on one channel, the output from the other channels was monitored. These outputs did not have the symmetry as did the other channel, because the spot was not centered on them. However, as the spot was moved about 0.6 mil, the output from this channel became symmetric and the amplitude was the same as the previous channel. In this fashion, the amplitude of the outputs was found to be extremely uniform as the spot was scanned from the right side to the left side, except for an area close to the output side of the TDI section. This initial moving spot optically demonstrates the multiplexing capability and provides qualitative data on the horizontal resolution of the 748x96-element TDI page reader with 4:1 multiplexing.

Both the horizontal and the vertical resolutions of the 748x96-element TDI array were demonstrated by illuminating the TDI array with optical test patterns produced by a strobe light. The light flashes were synchronized with the start of the TDI clocks. Thus, a strobe light occurred once a frame and the image could be entirely clocked out of the CCD before the strobe was flashed a second time. The test equipment setup for operating the 748x96-element TDI line sensor as a frame-transfer imager with a stroboscopic

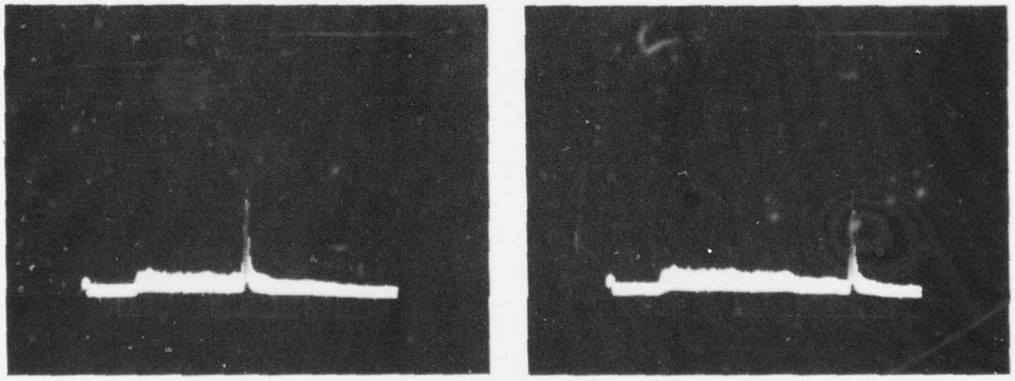


a.

No Spot

b.

Spot Focused on Right Side of the Chip



c.

Spot Focused near Chip Center

d.

Spot Focused near the Left Side of the Chip.

Figure 36. Test results from a scanning spot on the 748x96-element TDI-CCD page-reader test chip.

image is shown in Fig. 21. A TV-monitor image of one of the optical patterns used in these tests is shown in Fig. 37. The monitor used in a CONRAC TV monitor with a 12-inch diagonal screen. For these tests the output register clocks of the page-reader test array were adjusted to a TV compatible rate of about 3.3 MHz. The monitor picture in Fig. 37 reproduces only the output of one register. Therefore, it has only 25% (187 elements) of the resolution capability of the full array (748 elements). To demonstrate full horizontal resolution of the page-reader test array of 748 elements, the output of the four channels must be demultiplexed. This requires that the outputs of all four channels be sequentially sampled and displayed each line time until the full frame has been read out. Thus, the full 748x96-element field can be displayed in the form of four 187x96-element horizontally interlaced frames.

These tests clearly demonstrate the operation of the new concepts which are introducted in the 748x96-element TDI-CCD page-reader test chip with 4:1 multiplexing and show the feasibility of the 2200x96-element page reader.

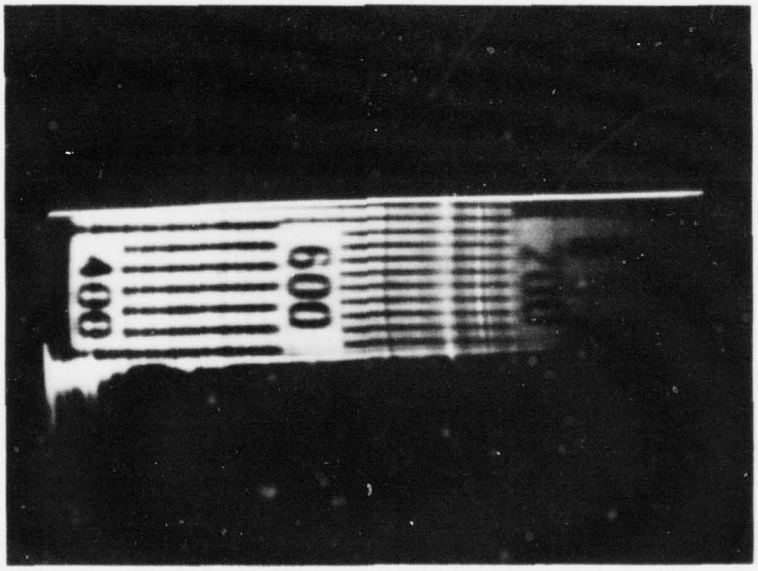


Figure 37. TV monitor picture illustrating the operation of the 748x96-element TDI-CCD page-reader test array with 4:1 multiplexed output. Single output channel is displayed (187 PELs) showing a standard line test pattern.

SECTION VI

CONCLUSIONS

A. NEW CCD STRUCTURES FOR HIGH-SPEED TDI PAGE READER

The new CCD imager design concepts incorporated in the 748x96-element page-reader test array are:

- electrode-per-bit clocking of the TDI array,
- serial output multiplexing, and
- high-speed TDI multiplexer

These new design concepts were conceived at RCA Laboratories to form the basis for design and development of a high-speed 2200x96-element TDI-CCD page reader for mail-scanning applications.

1. Electrode-Per-Bit Clocked TDI

A concept of using a electrode-per-bit clock for operating the TDI arrays has been developed and analyzed. With a four-phase ripple clock we can increases the vertical resolution by a factor of 1.5.

2. Serial Output Multiplexing

Several schemes have been developed for multiplexing the serial readout of the TDI sensor array. The output multiplexing allows improved horizontal resolution, as well as an increase in the effective serial scanning rate of the TDI array.

Two layouts for 4:1 output multiplexing with two-level polysilicon CCDs are included in the 748x96-element array, which has 0.6-mil x 0.6-mil picture elements (PELs). One layout, based on the use of four parallel registers with 2.4-mil stages, has been designed with wide design margins, but may have a limited frequency response. The second layout representing the high-speed approach to 4:1 multiplexing by means of two pairs of 2:1 multiplexed registers with 1.2-mil stages has been designed with more stringent design rules.

3. High-Speed TDI Multiplexer

A new charge-gating structure has been incorporated in the 748x96-element page-reader test array. With this new technique high-resolution 2:1 and 4:1 multiplexing of the TDI output can be achieved. Also to minimize the time required to load the four parallel output registers, the concept of a temporary line storage register has been introduced into the page-reader design.

B. RESULTS OBTAINED WITH 748x96 PAGE-READER TEST CHIP

The initial testing of the 748x96-element page-reader test chip has been completed, and the results have demonstrated that the concepts required for the 2200x96 full-size page reader are attainable. The tests have shown the following:

- The electrode-per-bit clock technique works (the increase in vertical resolution has not been tested).
- All multiplexing techniques work.
- The temporary storage concept works and allows faster loading into the output registers.
- The 748x96 array has vertical resolution and can be used in the TDI mode.
- Photocomposition of large chips is possible without significant degradation of the device characteristics.
- The process used was able to achieve 20% yield on one lot of wafers of 748x96-element page-reader sensors.

These results clearly indicate that the successful design and operation of the 2200x96-element array is possible.

C. WORK STILL REQUIRED ON THE PAGE-READER TEST CHIP

Further work required to fully evaluate the page-reader test chip to form solid foundation for the design of the full-size, high-speed 220x96-element TDI-CCD line sensor includes the following:

1. Device Processing

More processing runs of the page-reader test chip are needed to obtain about 50 bondable devices for futher study.

2. Testing and Evaluation of 748x96-Element Devices

Test equipment should be constructed to facilitate the electrical and optical testing of all the structures included on the 748x96-element test array. In addition to electrical and optical device testing to study operation and yield, this work should include the following tasks:

(a) Frequency response measurements should be made on the 4:1 and the double 2:1 multiplexed output registers for clock frequencies from 1 to 21 MHz. Based on these measurements a decision should be made as to which one of the two designs is the more suitable for the full-size, 2200x96-element TDI-CCD page reader.

(b) The 748x96-element TDI-CCD line sensor should be used to demonstrate that the specified performance of the high-speed TDI-CCD page-reader required by NOSC can be achieved. These specifications, including the uniformity of optical response and dark current, the dynamic range, and the output clock rate will be determined by electrical and stationary optical testing of the 748x96-element device. These tests can be performed by static strobe illumination tests of the TDI sensors. To display full 748-element horizontal resolution the four output frames can be displayed in horizontally interlaced mode.

(c) In the event the processing yield of the test arrays made with two-level polysilicon technology should be marginal when extrapolated for fabrication of acceptable full-size, 2200x96-element page-reader sensors, an evaluation should be made of the advantages of constructing the 2200x96-element TDI-CCD page-reader with the three-level polysilicon CCD technology.

To accomplish this, some wafer processing runs of the 748x96-element page-reader test chip must be made with the three-level polysilicon CCD technology.

3. Design and Cost Projection for the 2200x96-Element TDI-CCD Sensor

The 2200x96-element TDI-CCD line sensor should be designed on the basis of the accumulated data on the performance and yield of the 748x96-element page-reader test chips. Based on the accumulated data from the performance and yield of the page-reader test chips, a cost projection also can be made for fabricating the 2200x96-element page-reader devices which will meet the NOSC requirements for demonstrating the high-speed page-reader systems.